UltraZed-EG PCIe Carrier Card
Avnet Engineering Services
www.avnetkits.com

Sheet Name
01 - Avnet Lead Sheet
02 - Block Diagram
03 - PS - uSD, PMOD, LED, UARTs
04 - PS GTR - PCIe, SATA, USB
05 - PS GTR - DP
06 - Ref CLK
07 - PL - FMC LPC
08 - PL - User LEDs, Switches, Buttons & Touch Panel
09 - PL - PMODs
10 - SOM - GbE & MAC
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12 - SOM - JX1, JX2
13 - SOM - JX3
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AVNET® Reach Further™

UltraZed-EG PCIe Carrier Card

Revision: 1

AVNET® Avnet Engineering Services			
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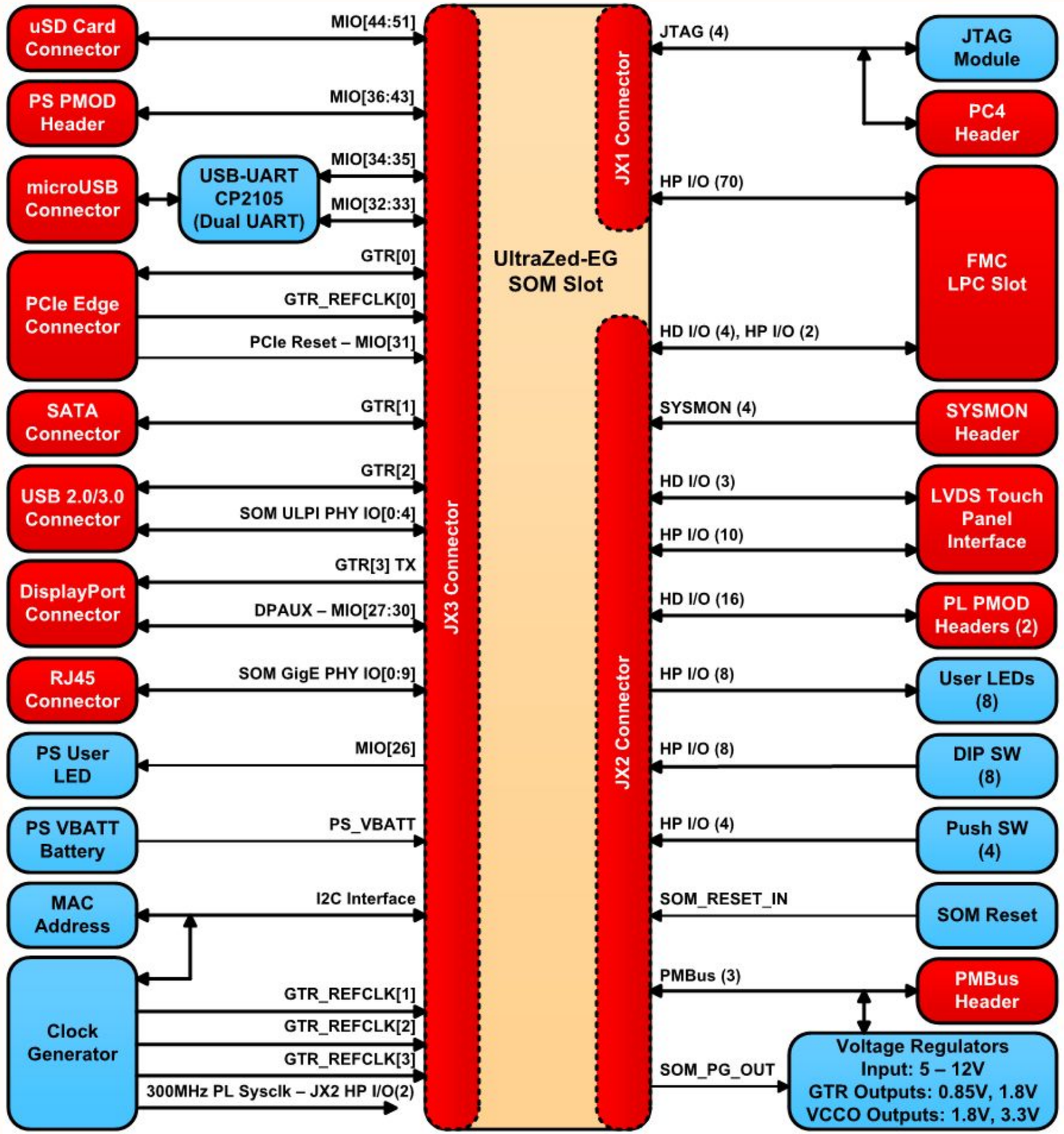
Doc Num: SCH-US2CAR	Date: 21/09/17	Time: 11:00:17 AM	
Sheet Title: 01 - Avnet Lead Sheet.SchDoc	Size: B	Sheet: 1 of 16	



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Project Name: UltraZed-EG PCIe Carrier Card	PCB Rev: 1	BOM: 01	Variant: 08
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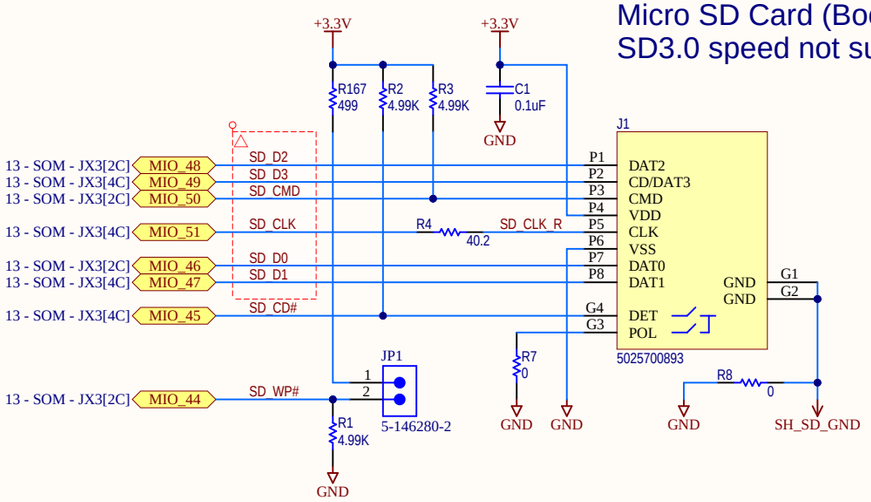
Sheet Title: 02 - Block Diagram.SchDoc	Size: B	Sheet: 2 of 16	

PS Bank501 MIO Interface: MicroSD, PMOD, LED & Dual-UART

Micro SD Card (Bootable)
SD3.0 speed not supported

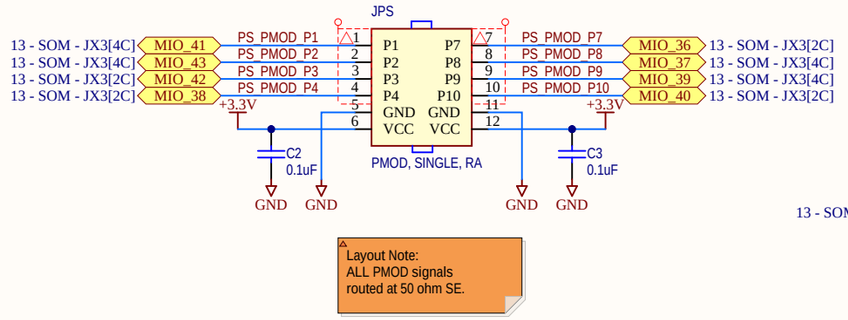


Layout Note:
Ensure a 50pS-200pS skew between CMD/Data and CLK.
Place R4 within 100 mils.

User's Note:
JP1: Leave open (default)
JP1: Short to emulate SD Write Protect.

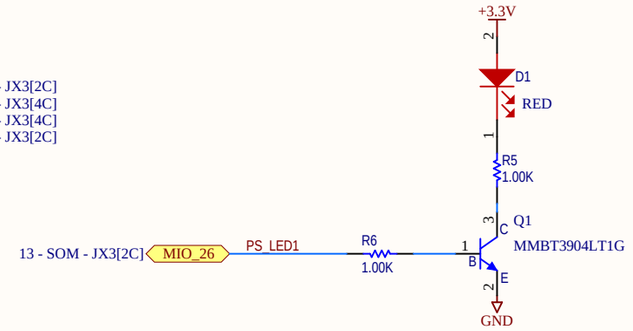
SH1

PS PMOD Interface

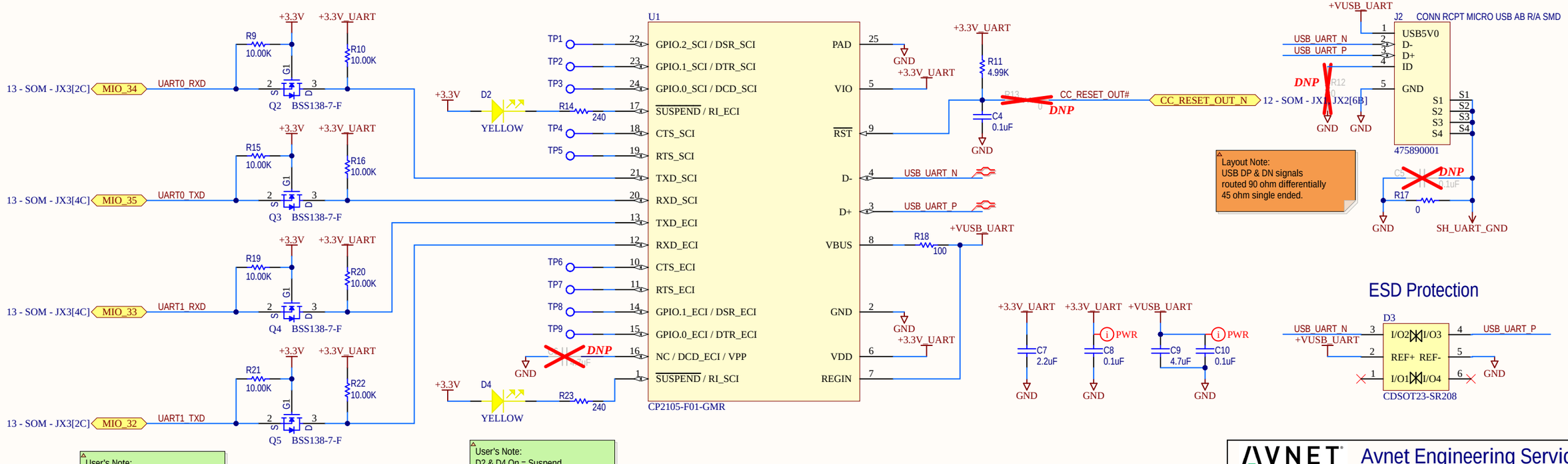


Layout Note:
ALL PMOD signals routed at 50 ohm SE.

PS User LED



Dual USB UART



User's Note:
TXD and RXD are swizzled on this interface to create null modem connections.

User's Note:
D2 & D4 On = Suspend

Layout Note:
USB DP & DN signals routed 90 ohm differentially 45 ohm single ended.

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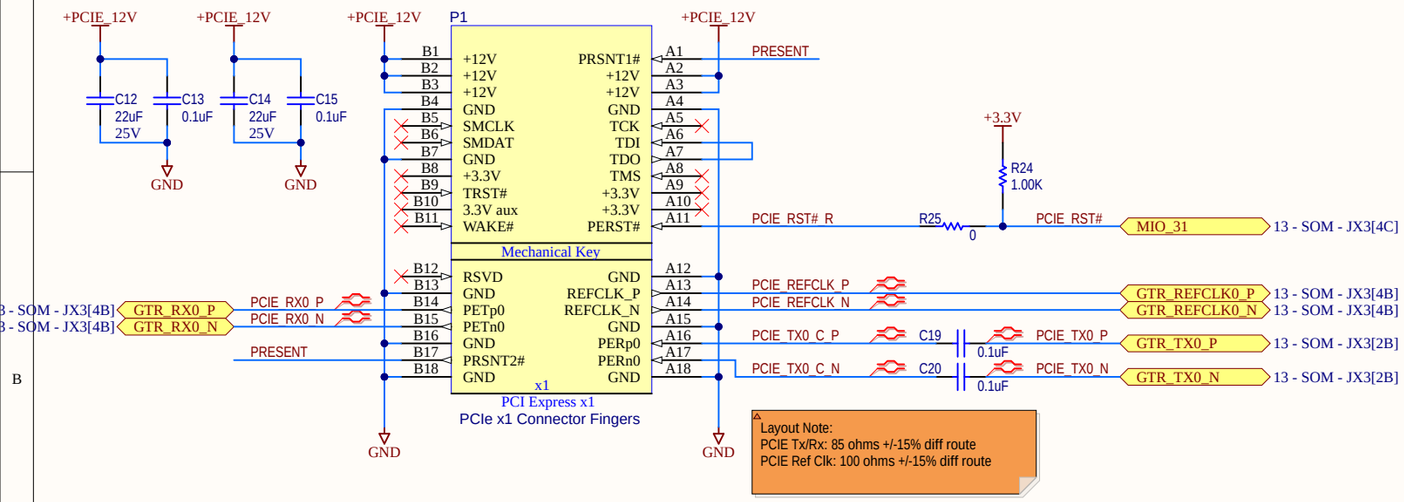
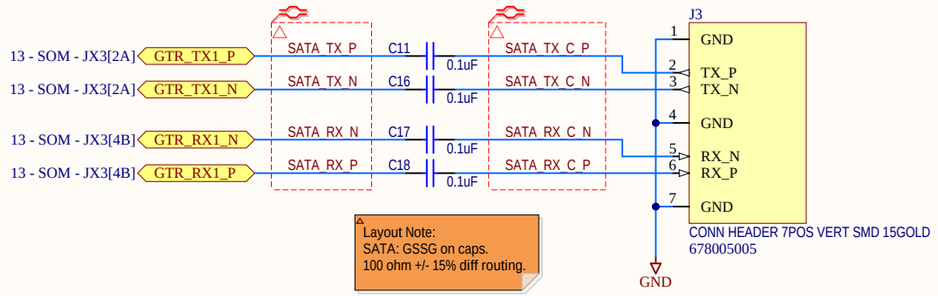
Sheet Title: 03 - PS - uSD, PMOD, LED, Uarts.SchDoc	Size: B	Sheet: 3 of 16		

PS GTR Interface #1: PCIe, SATA, USB

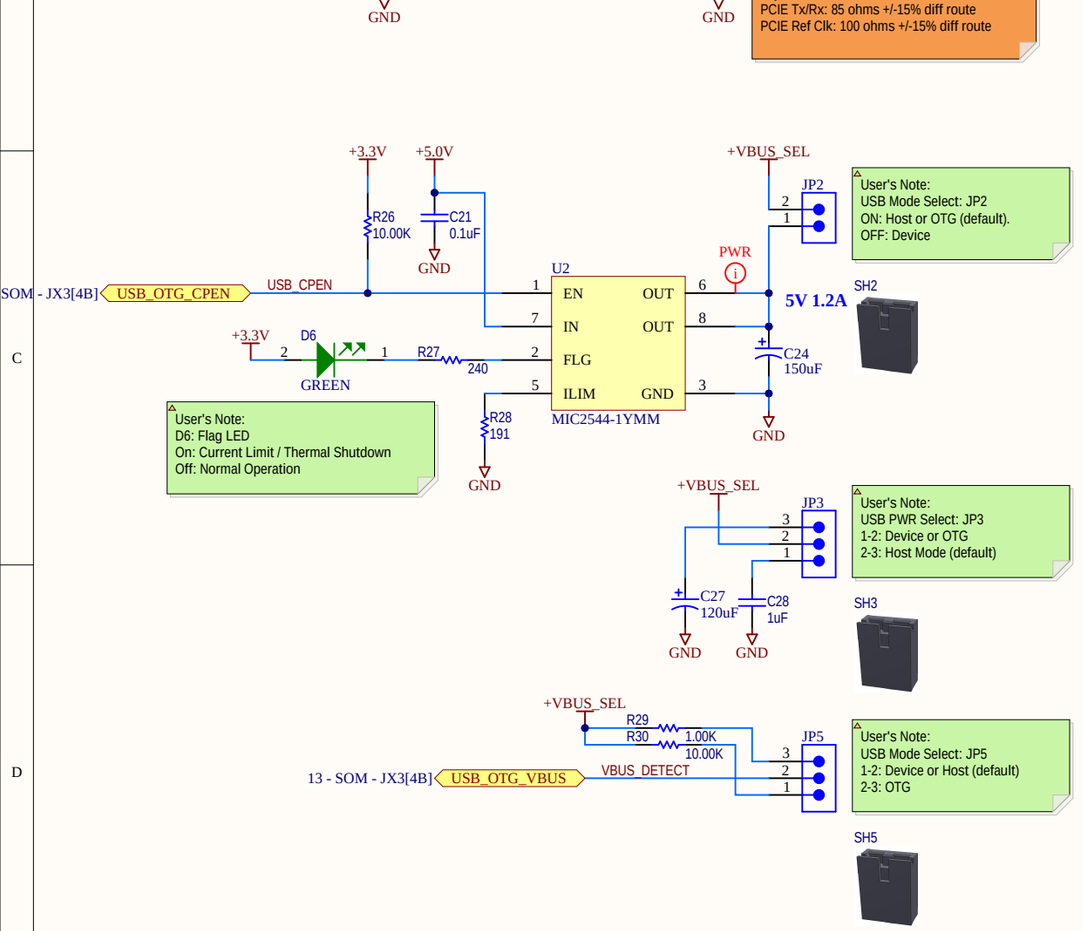
PCIe Gen2 Endpoint



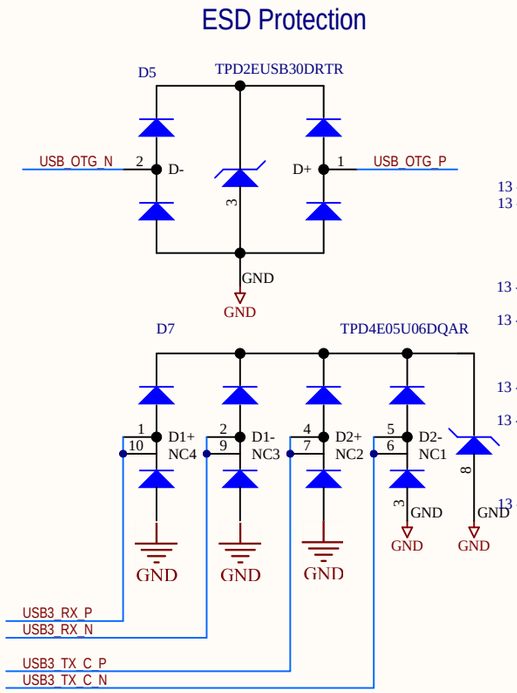
SATA Gen3 Host

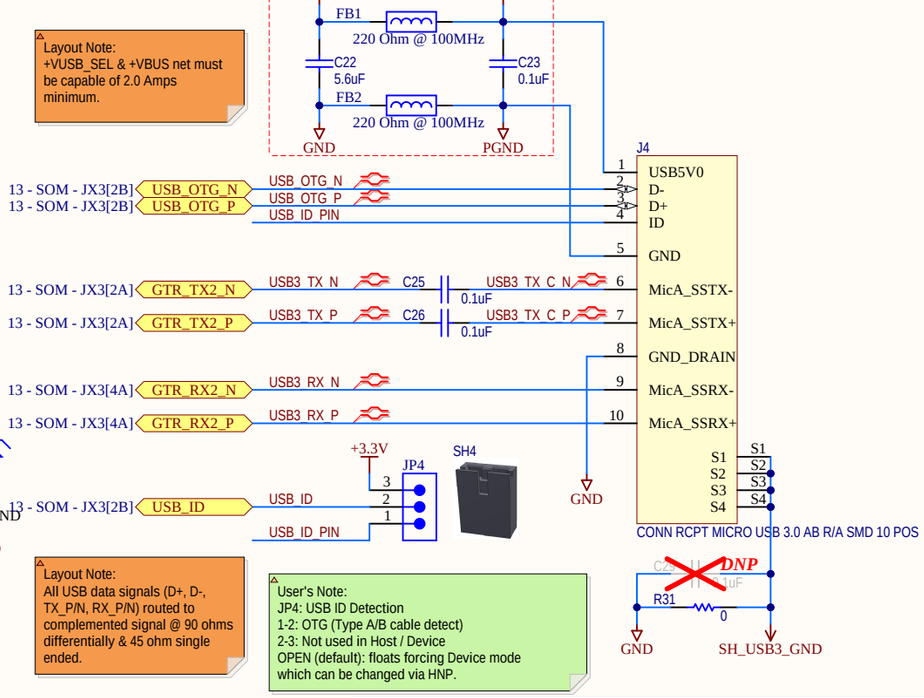


USB 2.0/3.0/OTG



ESD Protection





AVNET	Avnet Engineering Services
Project Name:	UltraZed-EG PCIe Carrier Card
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Sheet Title:	04 - PS GTR - PCIe, SATA, USB.SchDoc
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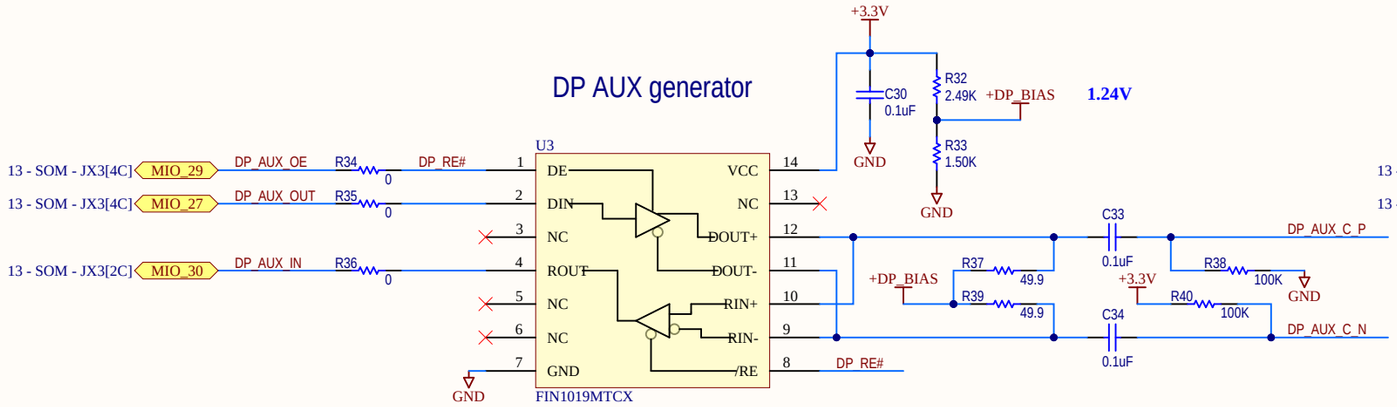
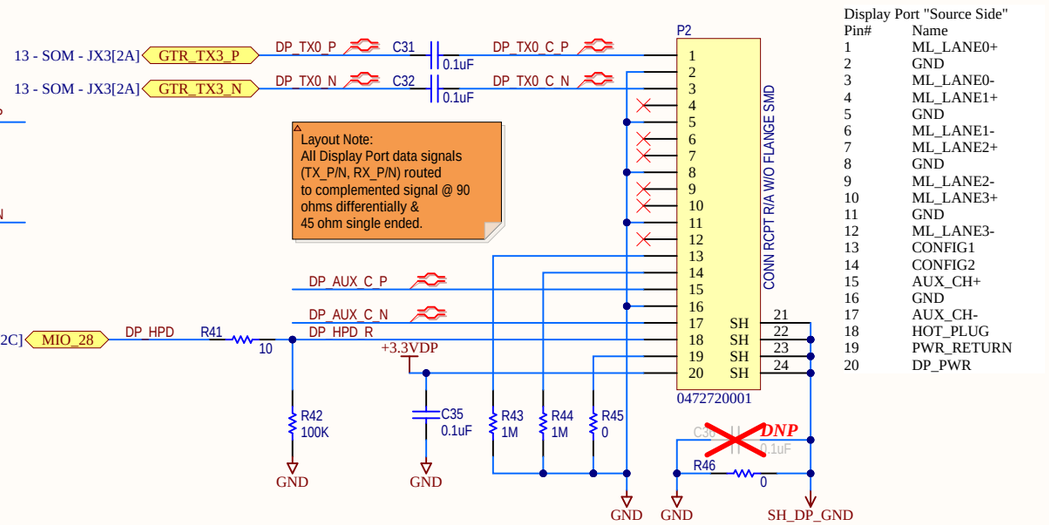
PS GTR Interface #2: DP

DP AUX generator



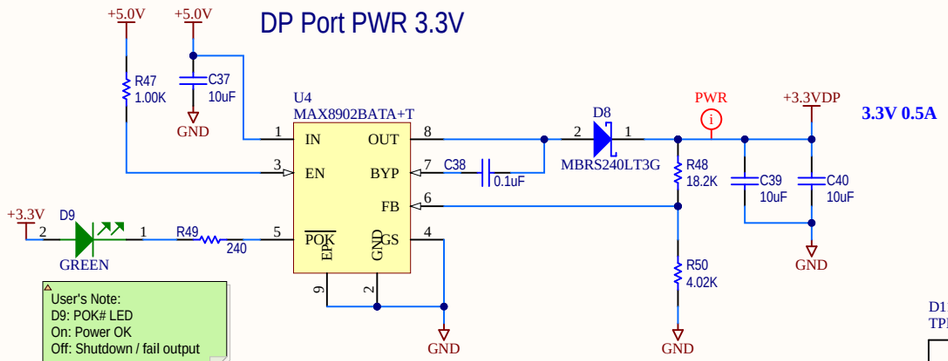
DP 1.2



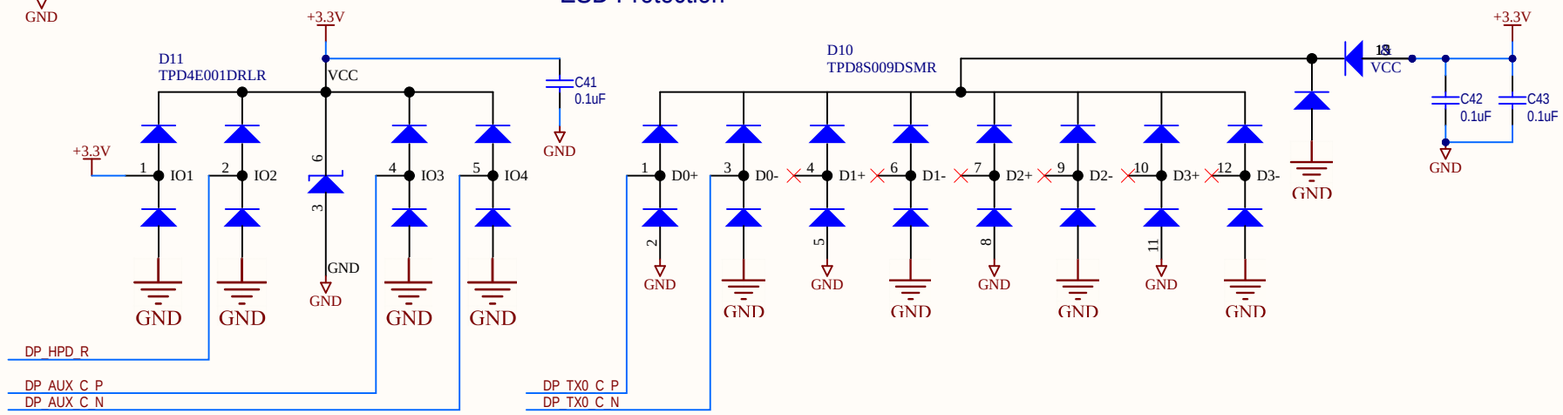
Display Port "Source Side"

Pin#	Name
1	ML_LANE0+
2	GND
3	ML_LANE0-
4	ML_LANE1+
5	GND
6	ML_LANE1-
7	ML_LANE2+
8	GND
9	ML_LANE2-
10	ML_LANE3+
11	GND
12	ML_LANE3-
13	CONFIG1
14	CONFIG2
15	AUX_CH+
16	GND
17	AUX_CH-
18	HOT_PLUG
19	PWR_RETURN
20	DP_PWR

DP Port PWR 3.3V



ESD Protection



Project Name:	Ultra Zed-EG PCIe Carrier Card
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Sheet Title:	05 - PS GTR - DP.SchDoc
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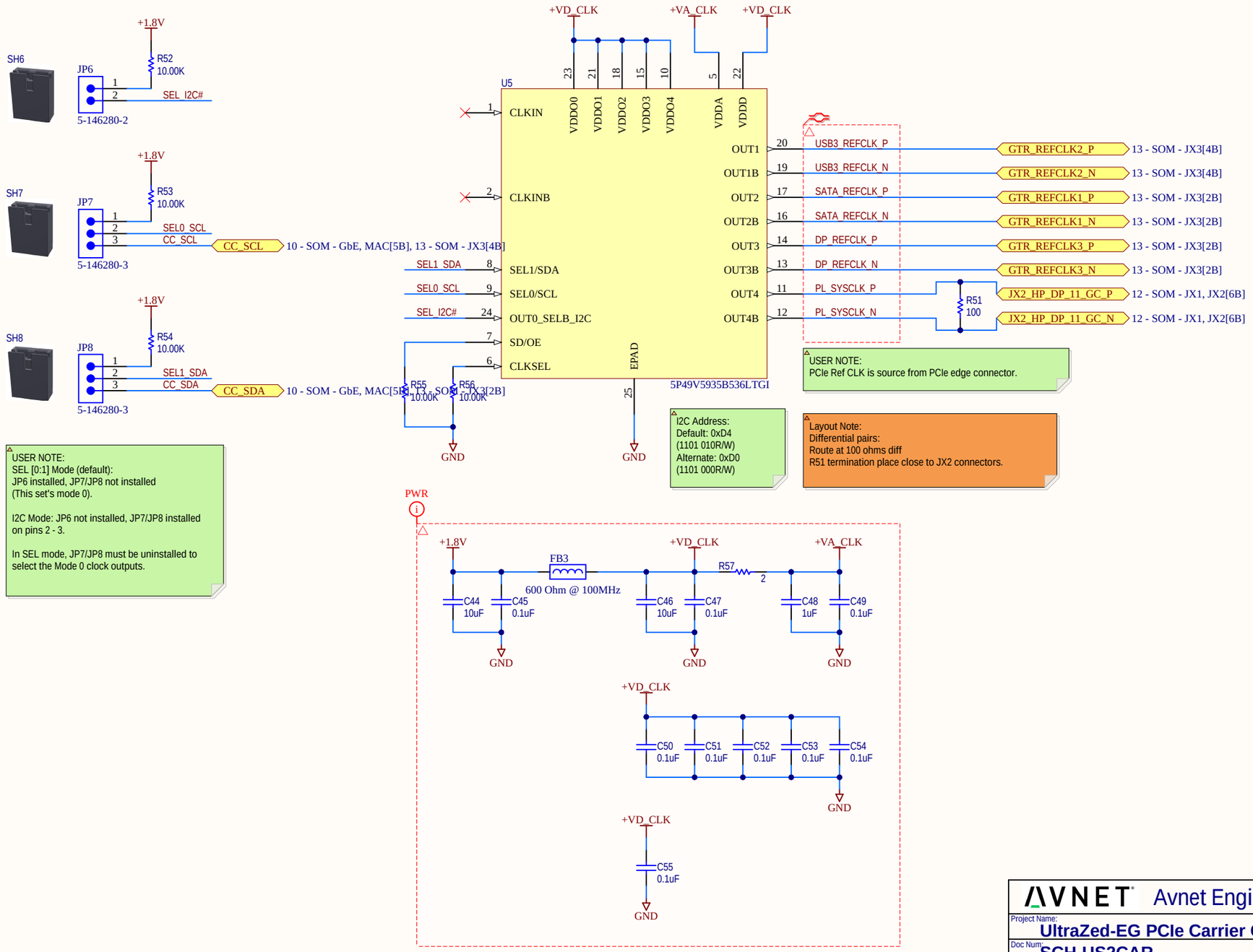
PS GTR & PL Ref Clock

IDT Clock Synthesizer



AVNET Avnet Engineering Services			
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FMC LPC (PL Bank64 & Bank65)

CON1A
Column C
ASP-134603-01

CON1B
Column D
ASP-134603-01

CON1C
Column G
ASP-134603-01

CON1D
Column H
ASP-134603-01

Layout Note:
FMC Differential Pairs
100 ohm +/- 15% diff routing.

SH9
SH10
JP10
JP11
5-146280-3

User's Note:
JP10 & JP11: FMC IPMI I2C Address Select.
Default: JP10 & JP11 pins 1-2.

CON1E
ASP-134603-01

CON1F
ASP-134603-01

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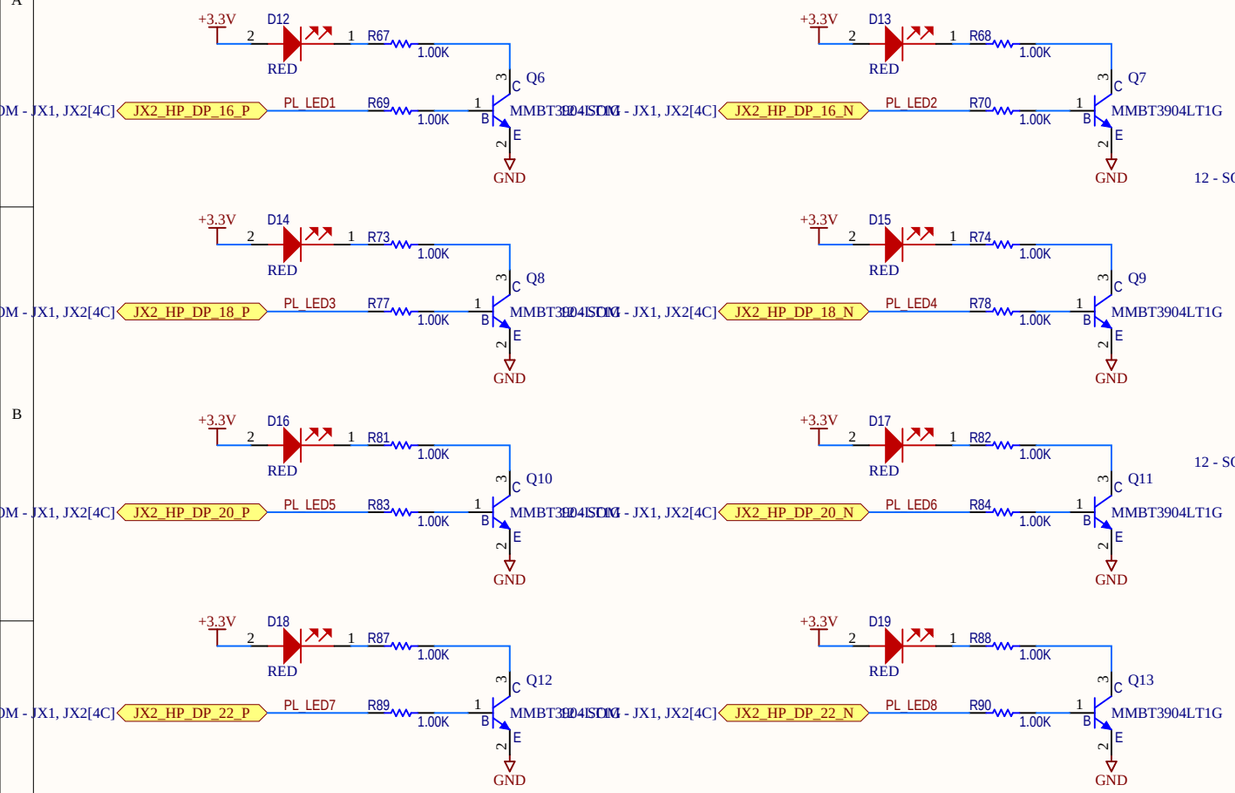
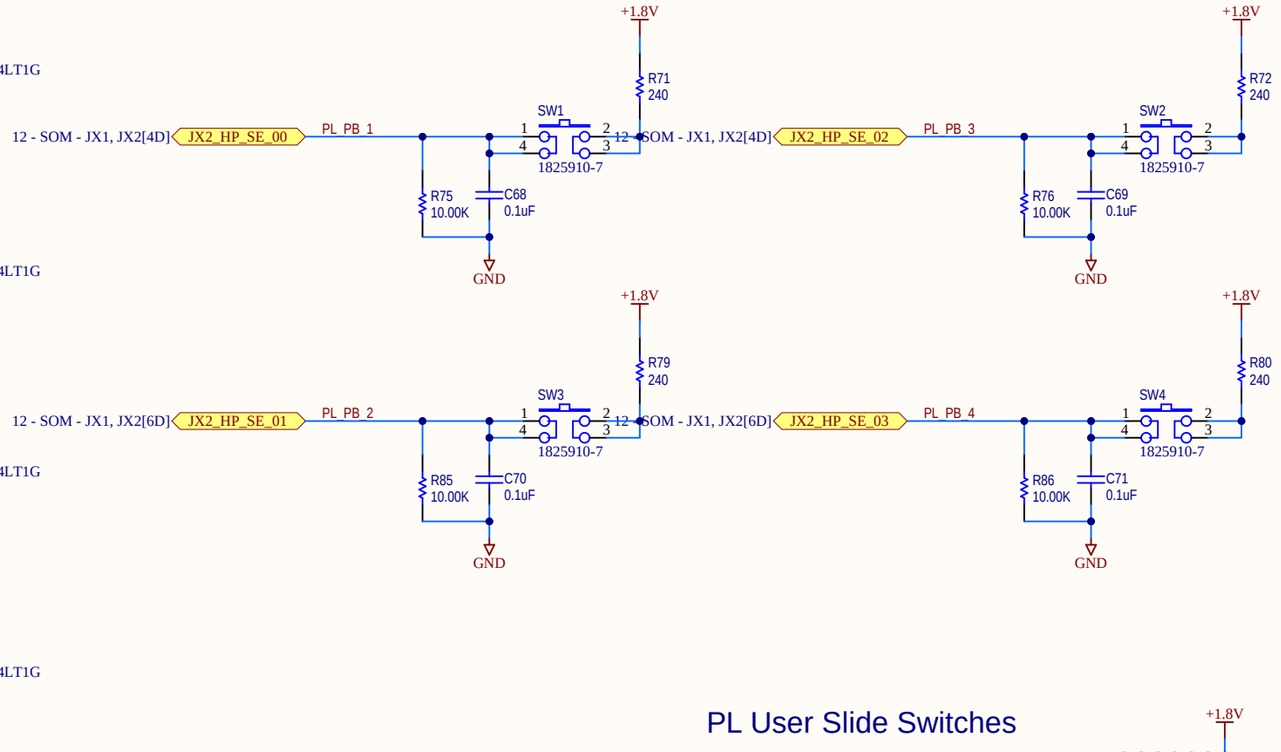
PL Bank66 (HP) I/O Perihperals: User LEDs / Slide Switches / Push Buttons & Touch Panel

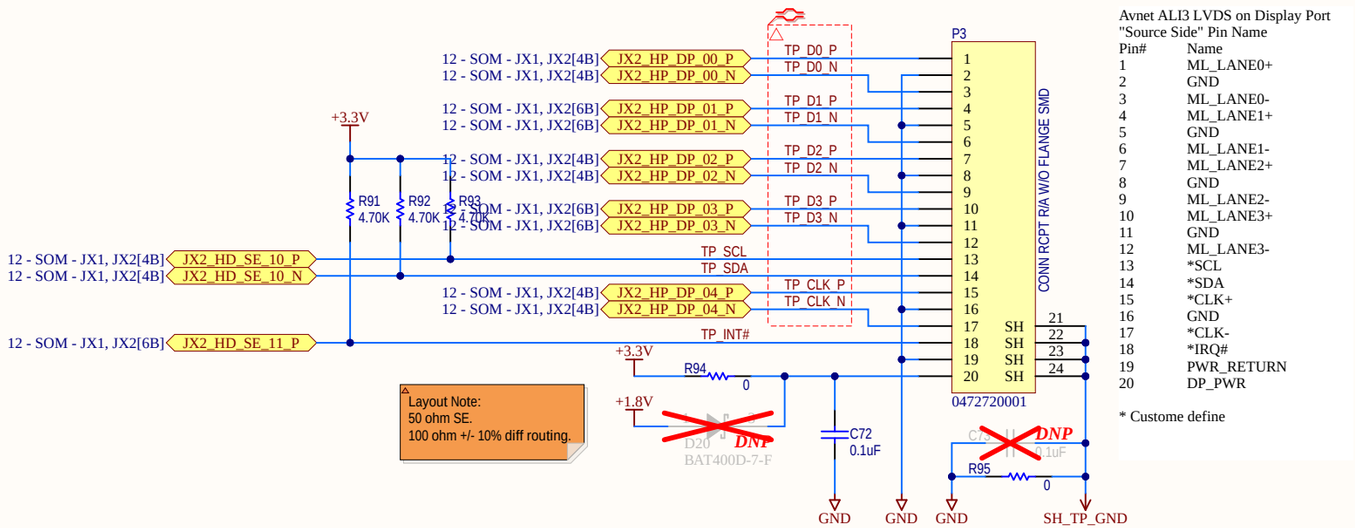
PL User LEDs



PL User Push Buttons



LVDS Touch Panel

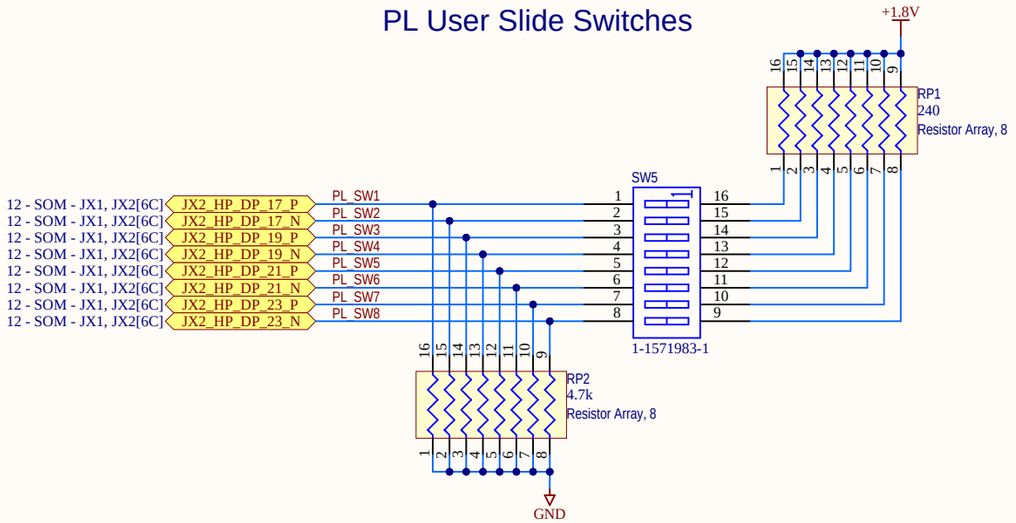


Avnet ALI3 LVDS on Display Port
"Source Side" Pin Name

Pin#	Name
1	ML_LANE0+
2	GND
3	ML_LANE0-
4	ML_LANE1+
5	GND
6	ML_LANE1-
7	ML_LANE2+
8	GND
9	ML_LANE2-
10	ML_LANE3+
11	GND
12	ML_LANE3-
13	*SCL
14	*SDA
15	*CLK+
16	GND
17	*CLK-
18	*IRQ#
19	PWR_RETURN
20	DP_PWR

* Custome define

PL User Slide Switches



Project Name:	Avnet Engineering Services
	UltraZed-EG PCIe Carrier Card
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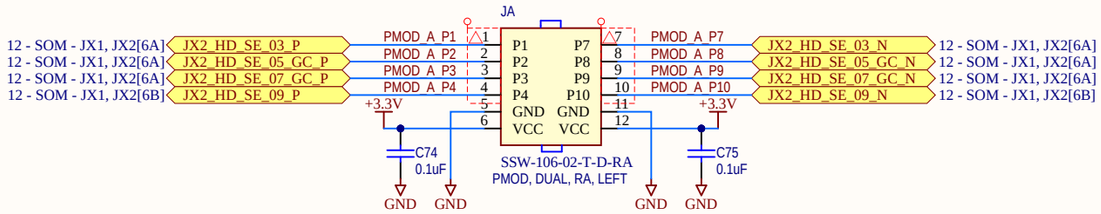
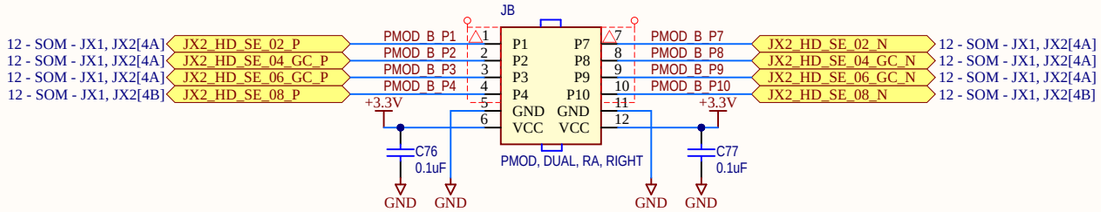
PL Bank26 (HD) I/O Perihperals: Dual PMOD

PL Dual PMOD

PMOD JA



PMOD JB



Layout Note:
ALL PMOD signals
routed at 50 ohm SE.

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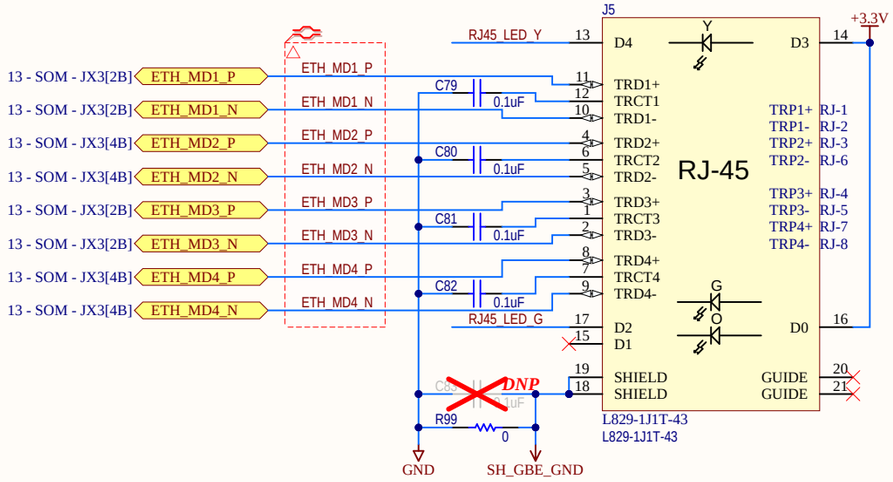
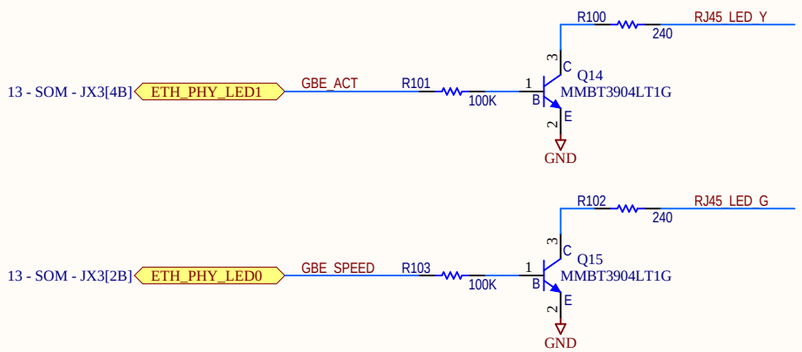
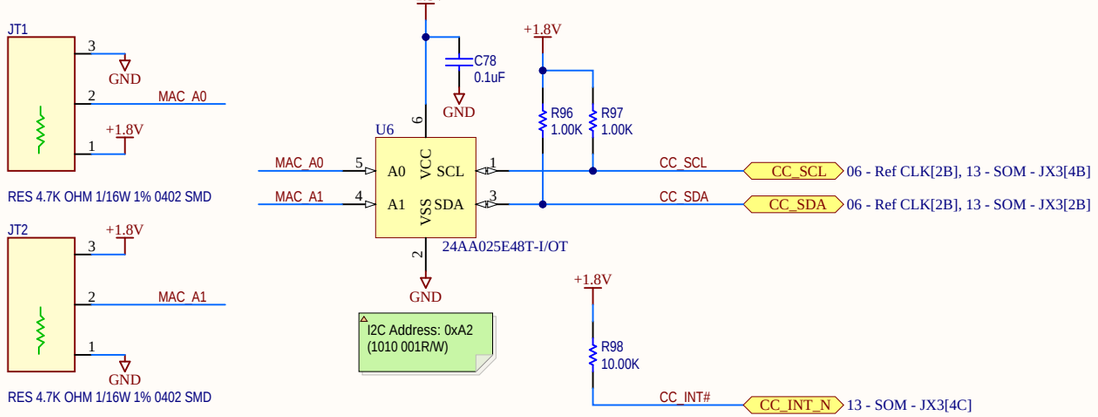
SOM GbE & MAC ID

SOM GbE





MAC ID - EEPROM



Avnet Engineering Services	
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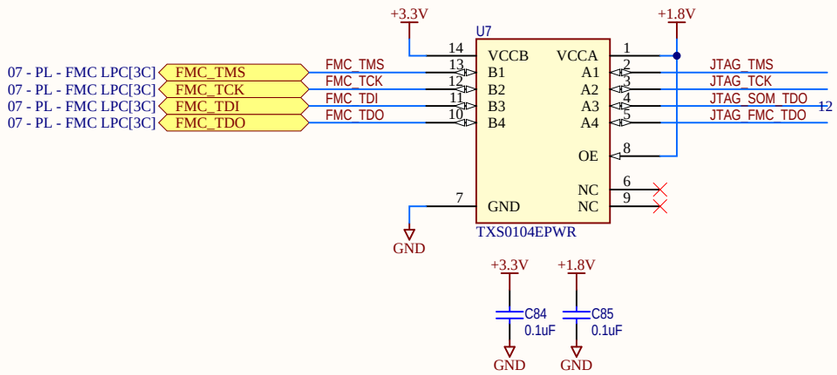
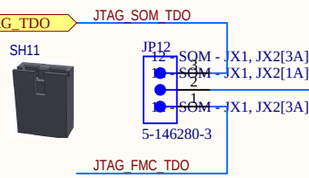
Sheet Title: 10 - SOM - GbE, MAC.SchDoc	Size: B / Sheet: 10 of 16

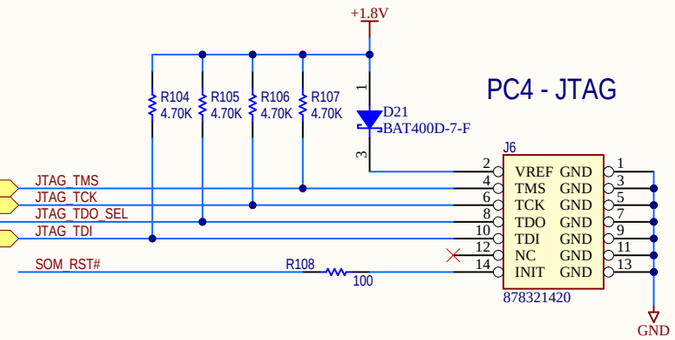
SOM Control & Analog In

JTAG Chain

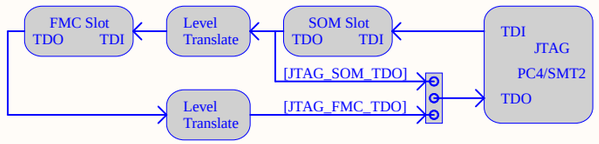
FMC JTAG Level Translate



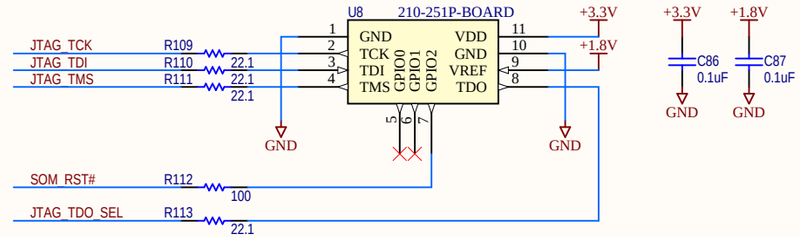




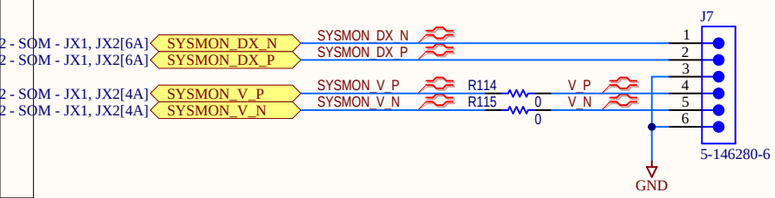
User's Note:
JP12: JTAG chain selection
1-2: JTAG pass through SOM & FMC
2-3: JTAG pass through SOM Only



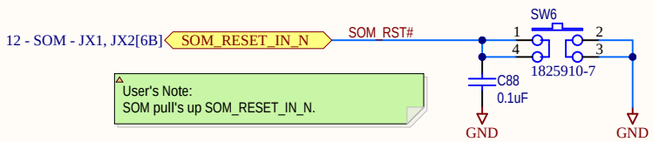
SMT2 USB-JTAG



SYSMON Header



SOM_RST_N



User's Note:
SOM pull's up SOM_RESET_IN_N.

AVNET Avnet Engineering Services			
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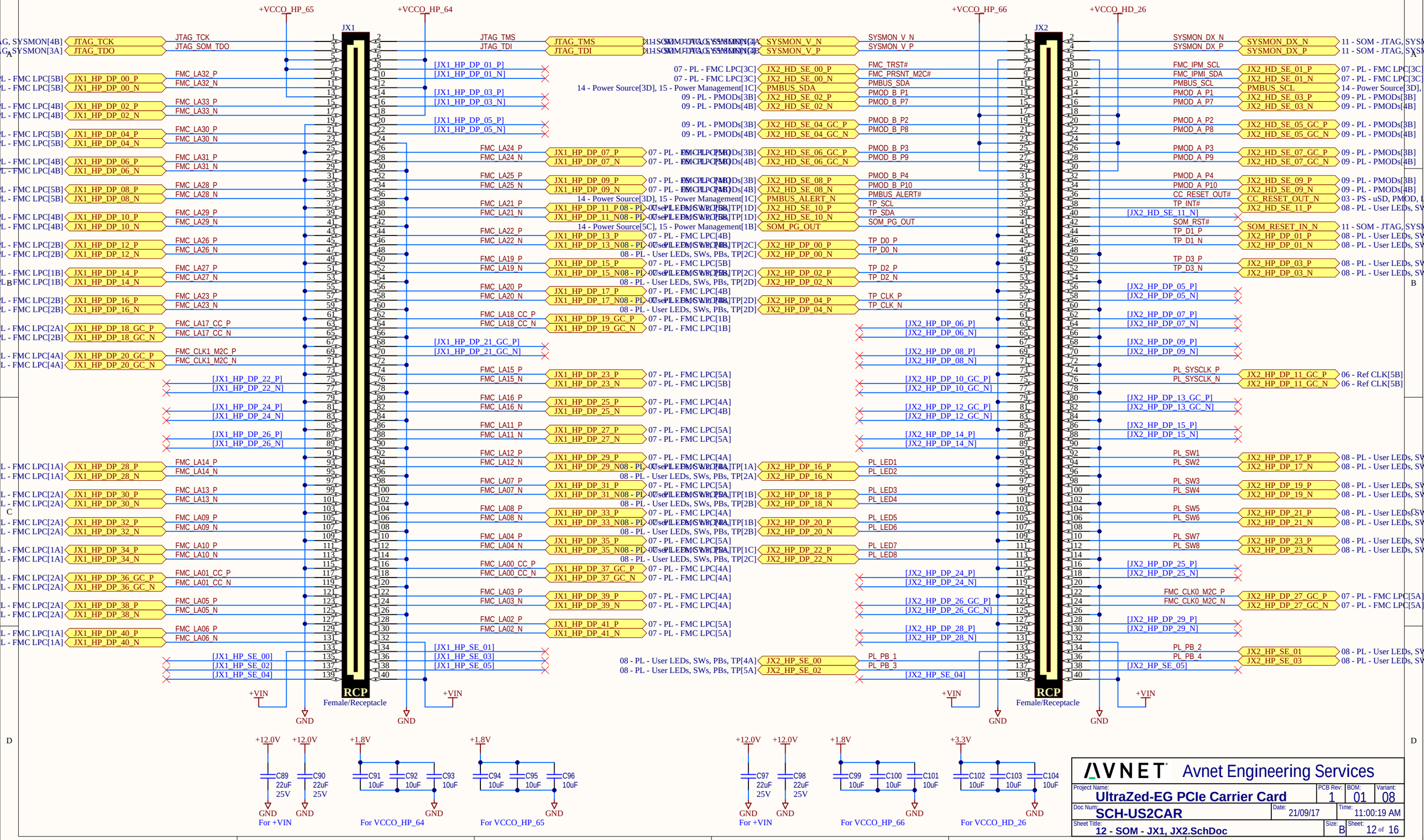
SOM JX1 & JX2



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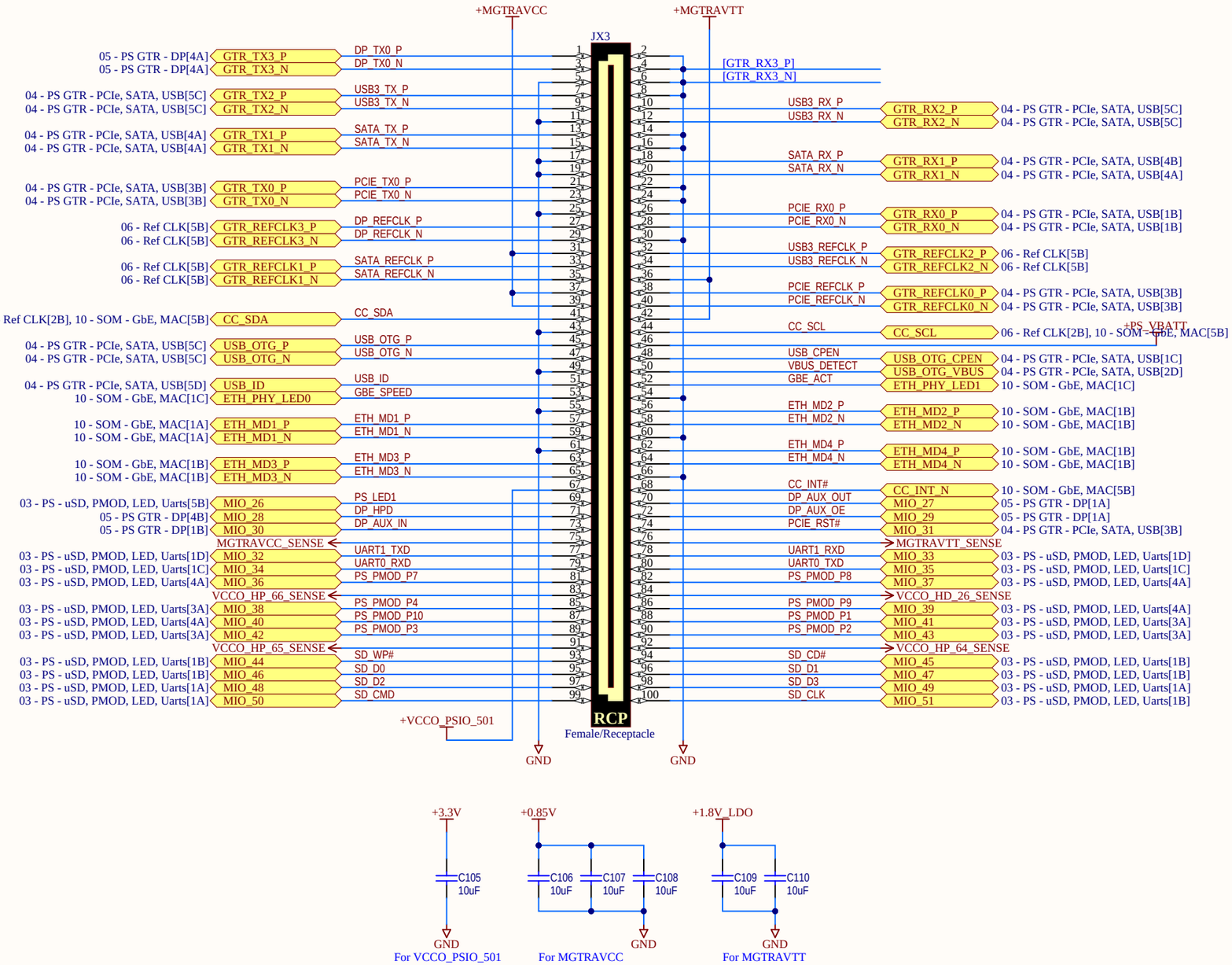
SOM JX3



AVNET Avnet Engineering Services

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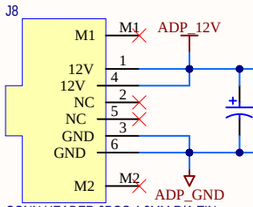
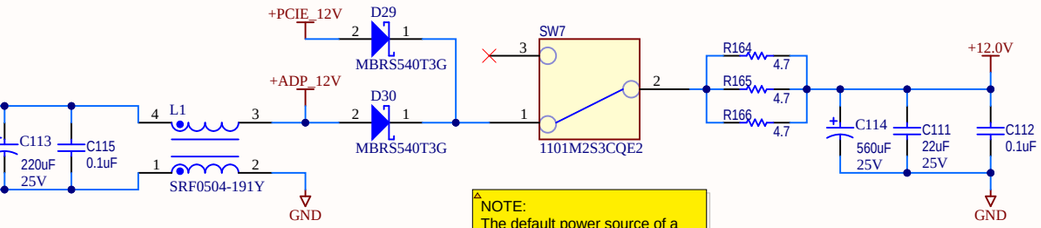
Power Source & Monitoring

PWR

Power Jack





User's Note:
For Xilinx 12V Adapter only.
Not compartible to ATX PCIe 6P connector.

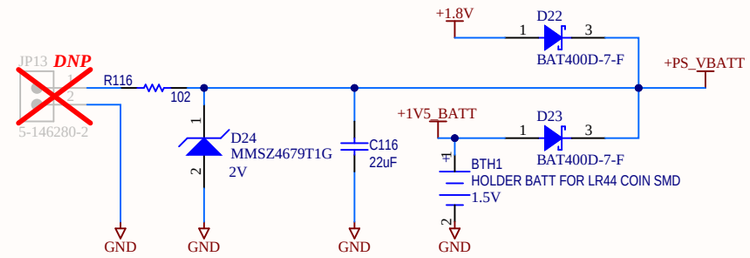
PCIe Card mode:
Must be powered by PCIe slot or using Xilinx 4P to 6P conversion cable.

Standalone mode:
Must be powered by Xilinx Adapter

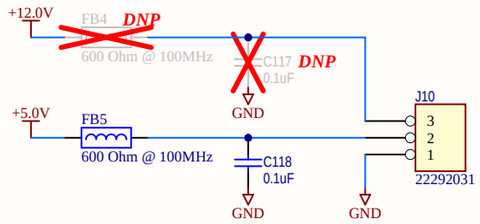
Main Power Switch

NOTE:
The default power source of a PCIe x1 slot is 10W per PCIe 1.1 specification. Extended is 25W via the PC's BIOS or SW OS configuration.

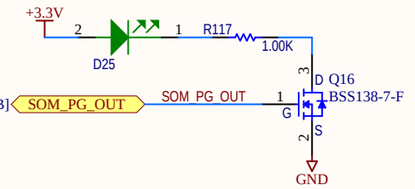
PS VBATT Options



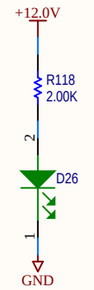
Fan Header



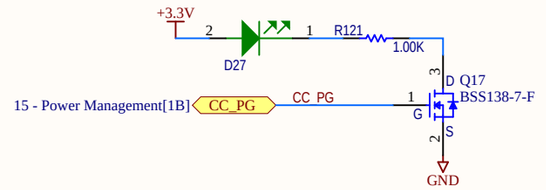
SOM Module PG



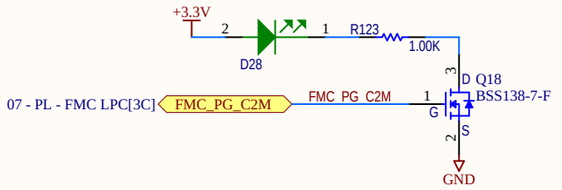
+12V Main Input

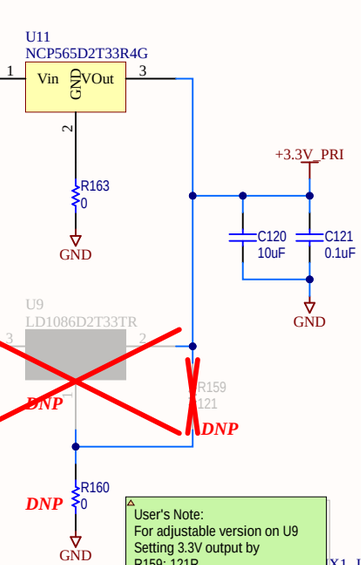


Carrier Card PG



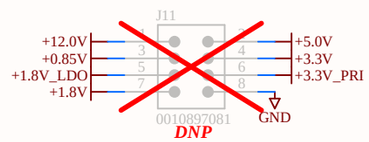
FMC PG C2M





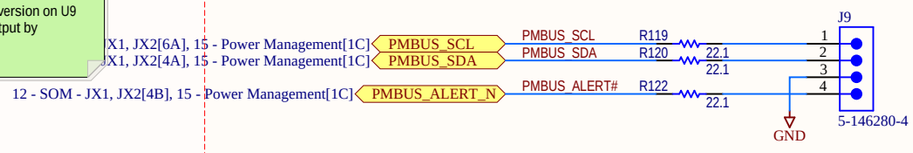
User's Note:
For adjustable version on U9
Setting 3.3V output by
R159: 121R
R160: 200R

Voltage Monitor Header



DNP

PMBus Header



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Power Management IC

PWR

U10
AVT~IRPS5401MTRPBF/BKN~461435~PMR

+12.0V +12.0V +12.0V +12.0V +12.0V +3.3V_PRI

49 VSUPPLY
39 VIN_A
32 VIN_B
12 VIN_C1
13 VIN_C2
14 VIN_C3
1 VIN_D1
2 VIN_D2
3 VIN_D3
22 VIN_LDO

INT_5V
R124 2
C122 4.7uF
C123 4.7uF
C125 4.7uF
AGND
GND

48 VCC
47 VDRV
21 1V8

42 EN_A
44 EN_B
51 EN_C
53 EN_D
28 EN_L

+3.3V_PRI
R125 10.00K DNP
, 14 - Power Source[5C] SOM_PG_OUT
R127 0
C130 0.1uF
R128 1M
GND

26 PG_A
30 PG_B
27 PG_C
16 PG_D
25 PG_L

+3.3V_PRI
R131 10.00K
14 - Power Source[5C] CC_PG
CC_PG

+3.3V_PRI
20 VDDIO

, 14 - Power Source[3D] PMBUS_SCL
PMBUS_SCL 18 CLK
, 14 - Power Source[3D] PMBUS_SDA
PMBUS_SDA 19 DATA
, 14 - Power Source[3D] PMBUS_ALERT_N
PMBUS_ALERT# 17 ALERT#

+3.3V_PRI
R139 10.00K
55 ADDR_PROT
52 SYNC_CLK
29 SLEEP#
54 MTP

R132 3.48K C151 10000pF AGND
R144 10.00K AGND
R134 3.48K C152 10000pF AGND
50 AGND
R146 0
57 GND

43 PWM_A
38 BOOT_A
36 PHASE_A1
37 PHASE_A2
46 ISEN_A+
45 ISEN_A-
40 RTN_A
41 FB_A
33 BOOT_B
34 PHASE_B1
35 PHASE_B2
31 FB_B
11 BOOT_C
8 PHASE_C1
9 PHASE_C2
10 PHASE_C3
15 FB_C
4 BOOT_D
5 PHASE_D1
6 PHASE_D2
7 PHASE_D3
56 FB_D
23 VO_LDO
24 FB_L

C124 0.1uF
L2 3.3µH 5A
+0.85V
C126 220uF C127 47uF C128 22uF C129 0.1uF
GND
0.85V 2A

FB_0V85
C131 0.1uF
L3 3.3µH 5A
+5.0V
C133 100uF C134 100uF C135 47uF C136 0.1uF
GND
5V 2A

FB_5V
C137 0.1uF
L4 3.3µH 5A
+3.3V
C138 220uF C139 47uF C140 22uF C141 0.1uF
GND
3.3V 4A

FB_3V3
C142 0.1uF
L5 1.5µH 6A
+1.8V
C144 220uF C145 47uF C146 22uF C147 0.1uF
GND
1.8V 4A

FB_1V8
C149 22uF C150 0.1uF
+1.8V_LDO
GND
1.8V 0.5A

+5.0V
R130 649
FB_5V
R133 649
GND

User's Note:
- I2C Address Offset +5
  (Set by R132 = 3.48K)
- MTP Bank# set by R134
- Switching Frequency: 1MHz

+3.3V_PRI +12.0V +12.0V +12.0V +12.0V +12.0V +3.3V_PRI
C153 0.1uF C154 1uF C155 22uF 25V C156 1uF C157 22uF 25V C158 1uF C159 47uF 25V C160 1uF C161 47uF 25V C162 1uF C163 22uF C164 1uF
GND

Layout Note:
Net Ties at 0.5mm each.
Tie as close as possible to each JX pin.

SOM Power Distribute

+12.0V +VIN
+3.3V +VCCO_HD_26
+1.8V +VCCO_HP_65
+0.85V +MGTRAVCC
+3.3V +VCCO_PSIO_501
+1.8V +VCCO_HP_64
+1.8V +VCCO_HP_66
+1.8V_LDO +MGTRAVTT

DC-DC Feedback Selection

+0.85V
DNP R126 0
FB_0V85
R129 10
FB6 220 Ohm @ 100MHz
MGTRAVCC_SENSE
C132 0.1uF
GND

+3.3V
DNP R135 0
FB_3V3
R136 649
R137 10
FB7 220 Ohm @ 100MHz
VCCO_HD_26_SENSE
R138 649
C143 0.1uF
GND

+1.8V
DNP R140 0
FB_1V8
R141 10
FB8 220 Ohm @ 100MHz
R142 0
VCCO_HP_64_SENSE
C148 0.1uF
GND
DNP R143 0
VCCO_HP_65_SENSE
DNP R145 0
VCCO_HP_66_SENSE

+1.8V_LDO
DNP R147 0
FB_1V8LDO
R148 649
R149 10
FB9 220 Ohm @ 100MHz
MGTRAVTT_SENSE
R150 249
C165 0.1uF
GND

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Assembly:

Label1
BD-XXXX-XXXXX-G
Label, Product

Label2
BD-XXXX-XXXXX-G
Label, Product

ESD1

ESD Bag

Label_ESD1

Label, ESD

Mechanicals:

FM1 FM2 FM3 FM4
Fiducial_Mark_40_80 Fiducial_Mark_40_80 Fiducial_Mark_40_80 Fiducial_Mark_40_80
FM5 FM6 FM7 FM8
Fiducial_Mark_40_80 Fiducial_Mark_40_80 Fiducial_Mark_40_80 Fiducial_Mark_40_80

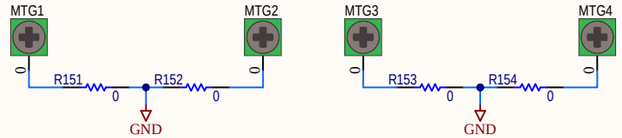
Mechanicals:

PCB

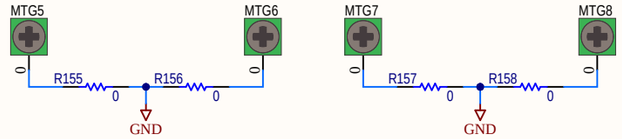
XXX-XXX-PCB-X

PCB PN (In Copper)

SOM Mounting Holes



Edge Stand-off Mounting Holes



Adhesive Bumper

BMPR1
BUMPER CYLIN 0.375" DIA BLK

BMPR2
BUMPER CYLIN 0.375" DIA BLK

BMPR3
BUMPER CYLIN 0.375" DIA BLK

BMPR4
BUMPER CYLIN 0.375" DIA BLK

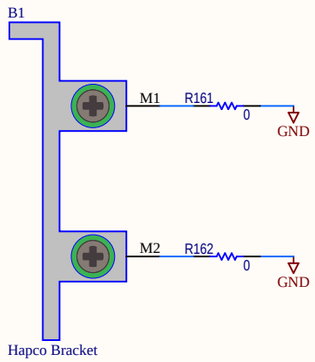
BMPR5
BUMPER CYLIN 0.375" DIA BLK

BMPR6
BUMPER CYLIN 0.375" DIA BLK

BMPR7
BUMPER CYLIN 0.375" DIA BLK

BMPR8
BUMPER CYLIN 0.375" DIA BLK

PCIe Card Bracket



Hapco Bracket

GND Test Pins

AVNET Avnet Engineering Services					
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