AR0144CS 1/4-inch 1.0 Mp CMOS Digital Image Sensor with Global Shutter

AR0144CS

ON Semiconductor®

www.onsemi.com

ODCSP69
CASE 570BV

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

Description

The AR0144CS is a 1/4-inch 1.0 Mp CMOS digital image sensor with an active-pixel array of 1280 (H) × 800 (V). It incorporates a new innovative global shutter pixel design optimized for accurate and fast capture of moving scenes. The sensor produces clear, low noise images in both low-light and bright scenes. It includes sophisticated camera functions such as auto exposure control, windowing, row skip mode, column-skip mode, pixel-binning and both video and single frame modes. It is programmable through a simple two-wire serial interface. The AR0144CS produces extraordinarily clear, sharp digital pictures, and its ability to capture both continuous video and single frames makes it the perfect choice for a wide range of applications, including scanning and industrial inspection.

Table 1. KEY PERFORMANCE PARAMETERS

Parameter	Typical Value
Optical Format	1/4-inch (4.5 mm)
Active Pixels	1280 (H) × 800 (V) = 1.0 Mp
Pixel Size	3.0 μm
Color Filter Array	RGB Bayer or Monochrome
Chief Ray Angle	0 or 20° or 28°
Shutter Type	Global Shutter
Input Clock Range	6–48 MHz
Output Pixel Clock (Maximum)	74.25 MHz
Output Serial Parallel	 MIPI, 1–lane or 2–lane 12-bit
Frame Rate Full Resolution 720p	 60 fps (Parallel, MIPI 2–lane, 12–bit) 44 fps (MIPI 1–lane, 12–bit) 52 fps (MIPI 1–lane, 10–bit) 66 fps (Parallel, MIPI 2–lane, 12–bit)
Responsivity Monochrome Color	 56 Ke/lux*s 22.3 ke–/lux*s
SNR_{MAX}	38 dB
Dynamic Range	71.4 dB
Supply Voltage I/O Digital Analog	 1.8 or 2.8 V 1.2 V 2.8 V
Power Consumption	< 215 mW
Operating Temperature	–40°C to + 85°C (Ambient) –40°C to + 105°C (Junction)
Package Options	5.6 × 5.6 mm 69-ball CSP
	Bare Die

Features

- Superior Low-light and IR Performance
- HD Video (720p60)
- 1/2–lane MIPI or Parallel Data Interface
- Automatic Black Level Calibration (ABLC)
- Programmable Control for Region Of Interest (ROI)
- Horizontal and Vertical Mirroring, Windowing and Pixel Binning
- On-chip Auto Exposure Control for Any Programmable ROI
- 5 × 5 Statistics Engine for Any Programmable ROI
- Flexible Control for Row and Column Skip Mode
- On-chip Trigger Mode for Synchronization
- Built in Strobe Control
- On Chip Phase Lock Loop (PLL)

Applications

- Bar Code Scanner
- Gesture Recognition
- 3D Scanning
- Positional Tracking
- Iris Scanning
- Augmented Reality
- Virtual Reality
- Biometrics
- Machine Vision

ORDERING INFORMATION

Table 2. AVAILABLE PART NUMBERS

Part Number	Product Description	Orderable Product Attribute Description
AR0144CSSC00SUKA0−CPBR	Color, CSP	RGB − CSP; CRA = 0; with Protective Film, Double Side BBAR Glass
AR0144CSSC00SUKA0−CRBR	Color, CSP	RGB − CSP; CRA = 0; without Protective Film, Double Side BBAR Glass
AR0144CSSC00SUKAH3−GEVB	Color, CSP	Head Board RGB − Headboard; CRA = 0
AR0144CSSC00SUD20	Color, Bare Die	RGB; CRA = 0
AR0144CSSM00SUKA0−CPBR	Mono, CSP	MONO − CSP; CRA = 0; with Protective Film, Double Side BBAR Glass
AR0144CSSM00SUKA0−CRBR	Mono, CSP	MONO − CSP; CRA = 0; without Protective Film, Double Side BBAR Glass
AR0144CSSM00SUKAH3−GEVB	Mono, CSP Head Board	MONO − Headboard; CRA = 0
AR0144CSSM00SUD20	Mono, Bare Die	MONO; CRA = 0
AR0144CSSC20SUKA0−CPBR	Color, CSP	RGB − CSP; CRA = 20; with Protective Film, Double Side BBAR Glass
AR0144CSSC20SUKA0−CRBR	Color, CSP	RGB − CSP; CRA = 20; without Protective Film, Double Side BBAR Glass
AR0144CSSC20SUKAH3−GEVB	Color, CSP Head Board	RGB − Headboard; CRA = 20
AR0144CSSC20SUD20	Color, Bare Die	Color, Bare Die
AR0144CSSM20SUKA0−CPBR	Mono, CSP	MONO − CSP; CRA = 20; with Protective Film, Double Side BBAR Glass
AR0144CSSM20SUKA0−CRBR	Mono, CSP	MONO − CSP; CRA = 20; without Protective Film, Double Side BBAR Glass
AR0144CSSM20SUKAH3−GEVB	Mono, CSP Head Board	MONO − Headboard; CRA = 20
AR0144CSSM20SUD20	Mono, Bare Die	MONO; CRA = 20
AR0144CSSM28SUKA0−CPBR	Mono, CSP	MONO − CSP; CRA = 28; with Protective Film, Double Side BBAR Glass
AR0144CSSM28SUKA0−CPBR1	Mono, CSP	MONO − CSP; CRA = 28; with Protective Film, MOQ = 1, Double Side BBAR Glass
AR0144CSSM28SUKA0−CRBR	Mono, CSP	MONO − CSP; CRA = 28; without Protective Film, Double Side BBAR Glass
AR0144CSSM28SUD20	Mono, Bare Die	MONO; CRA = 28

See the ON Semiconductor Device Nomenclature document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

GENERAL DESCRIPTION

The ON Semiconductor AR0144CS can be operated in its default mode or programmed for frame size, exposure, gain, and other parameters. The default mode output is a full-resolution image at 60 frames per second (fps). It outputs 12-bit raw data, using either the parallel or serial (MIPI) output ports. The device may be operated in video (master) mode or in frame trigger mode.

FRAME_VALID and LINE_VALID signals are output on dedicated pins, along with a synchronized pixel clock. A dedicated FLASH pin can be programmed to control external LED or flash exposure illumination.

The AR0144CS includes additional features to allow application-specific tuning: windowing, adjustable auto-exposure control, auto black level correction, on-board temperature sensor, row-skip and column-skip modes and binning modes.

The sensor is designed to operate in a wide temperature range (–40°C to +85°C).

FUNCTIONAL OVERVIEW

The AR0144CS is a progressive-scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on-chip, phase-locked loop (PLL) that can be optionally enabled to generate all internal clocks from a single master input clock running between 6 and 48 MHz. The maximum output pixel rate is 74.25 Mp/s, corresponding to a clock rate of 74.25 MHz. Figure 1 shows a block diagram of the sensor.

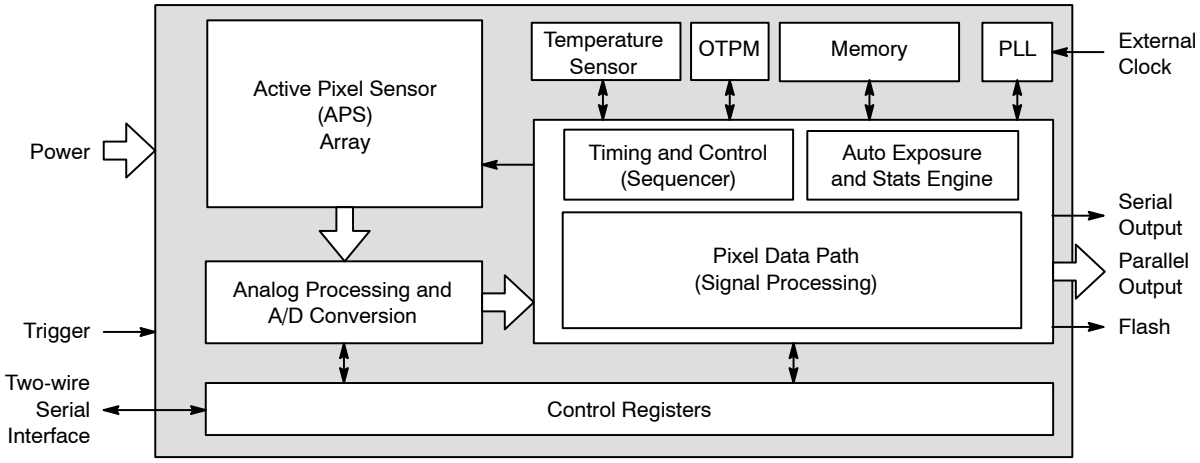


Figure 1. Block Diagram

User interaction with the sensor is through the two-wire serial bus, which communicates with the array control, analog signal chain, and digital signal chain. The core of the sensor is a 1.0 Mp Active-Pixel Sensor array. The AR0144CS features global shutter technology for accurate capture of moving images. The exposure of the entire array is controlled by programming the integration time by register setting. All rows simultaneously integrate light prior to readout. Once a row has been read, the data from the columns is sequenced through an analog signal chain (providing offset correction and gain), and then through an analog-to-digital converter (ADC). The output from the ADC is a 12-bit value for each pixel in the array. The ADC output passes through a digital processing signal chain (which provides further data path corrections and applies digital gain). The pixel data are output at a rate of up to 74.25 Mp/s, in parallel to frame and line synchronization signals.

FEATURES OVERVIEW

The AR0144CS Global Shutter sensor has a wide array of features to enhance functionality and to increase versatility. A summary of features follows. Please refer to the AR0144 Developer Guide for detailed feature descriptions, register settings, and tuning guidelines and recommendations.

- 3.0 μm Global Shutter Pixel
  To improve the low light performance and to capture the moving images accurately a large (3.0 μm) global shutter pixel is implemented for better image optimization.
- Operating Modes
  The AR0144CS works in master (video), trigger (single frame), or Auto Trigger modes. In master mode, the sensor generates the integration and readout timing. In trigger mode, it accepts an external trigger to start exposure, then generates the exposure and readout timing. The exposure time is programmed through the two-wire serial interface for both modes.
- Window Control
  Configurable window size and blanking times allow a wide range of resolutions and frame rates. Digital binning and skipping modes are supported, as are vertical and horizontal mirror operations.
- Frame Rate
  AR0144CS is capable of running up to 60 fps at full (1280 × 800) resolution and 66 fps at 720p resolution.
- Embedded Data and Statistics
  The AR0144CS has the capability to output image data and statistics embedded within the frame timing.
- Multi-Camera Synchronization
  The AR0144CS supports advanced line synchronization controls for multi-camera (stereo) support.
- Trigger Mode
  The trigger mode feature of the AR0144CS supports triggering the start of a frame readout from an input signal that is supplied from an external source.
  The trigger mode signal allows for precise control of frame rate and register change updates.
- Context Switching and Register Updates
  Context switching may be used to rapidly switch between two sets of register values.
  Refer to the AR0144 Developer Guide for a complete description of context switchable registers.
- Gain
  A programmable analog gain of 1x to 16x applied globally to all color channels is available along with a digital gain of 1x to 16x that may be configured on a per color channel basis.
- Automatic Exposure Control
  The integrated automatic exposure control may be used to ensure optimal settings of exposure and gain are computed and updated every other frame. Refer to the AR0144 Developer Guide for more details.
- MIPI
  The AR0144CS Global Shutter image sensor supports one or two lanes of MIPI data. Compliant to MIPI standards:
  - MIPI Alliance Standard for CSI−2 version 1.2
  - MIPI Alliance Standard for D−PHY version 1.0
- PLL
  An on chip PLL provides reference clock flexibility and supports spread spectrum sources for improved EMI performance.
- Reset
  The AR0144CS may be reset by a register write, or by a dedicated input pin.
- Output Enable
  The AR0144CS output pins may be tri-stated using a dedicated output enable pin.
- Temperature Sensor
- Black Level Correction
- Row Noise Correction
- Test Patterns
  Several test patterns may be enabled for debug purposes. These include a solid color, color bar, fade to gray, and a walking 1s test pattern.
- Silicon/OTPM Revision Information
  A revision register is provided to read out (via I^2C) silicon and OTPM revision information. This will be helpful to distinguish material if there are future OTPM or silicon revisions.
- Lens Shading Correction
  A lens shading correction algorithm is included for potential low Z height applications.
- Compression
  AR0144CS can optionally compress 12-bit data to 10-bit using A-law compression.

PIXEL DATA FORMAT

Pixel Array Structure

The AR0144CS pixel array is configured as 1484 columns by 856 rows, (see Figure 2). The dark pixels are optically black and are used internally to monitor black level. Of the left 180 columns, 168 are dark pixels used for row noise correction. Of the bottom 32 rows of pixels, 8 of the dark rows are used for black level correction. There are 1300 columns by 820 rows of optically active pixels. While the sensor's format is 1280 × 800, the additional active columns and active rows are included for use when horizontal or vertical mirrored readout is enabled, to allow readout to start on the same pixel. The pixel adjustment is always performed for monochrome or color versions. The central 1288 × 808 pixel active area is surrounded with optically transparent dummy pixels and non-optically transparent barrier pixels to improve image uniformity within the active area. Not all barrier pixels can be read out. The optical center of the readable active pixels can be found between X_ADDR 649 and 650, and between Y_ADDR 409 and 410.

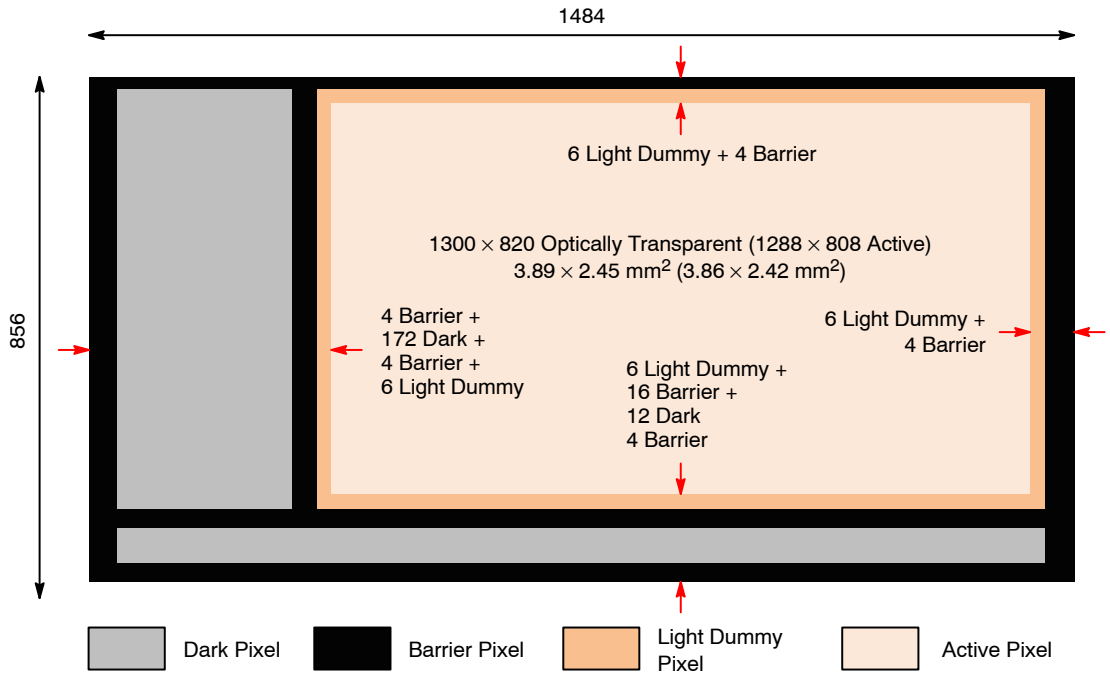


Figure 2. Pixel Array Description

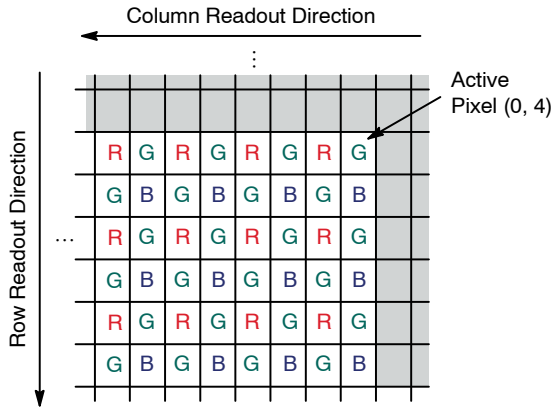


Figure 3. Pixel Color Pattern Detail (Top Right Corner)

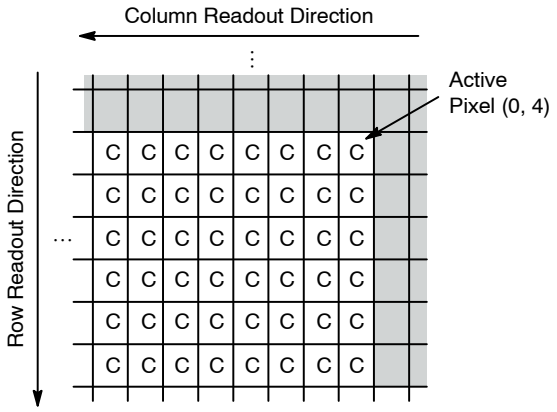


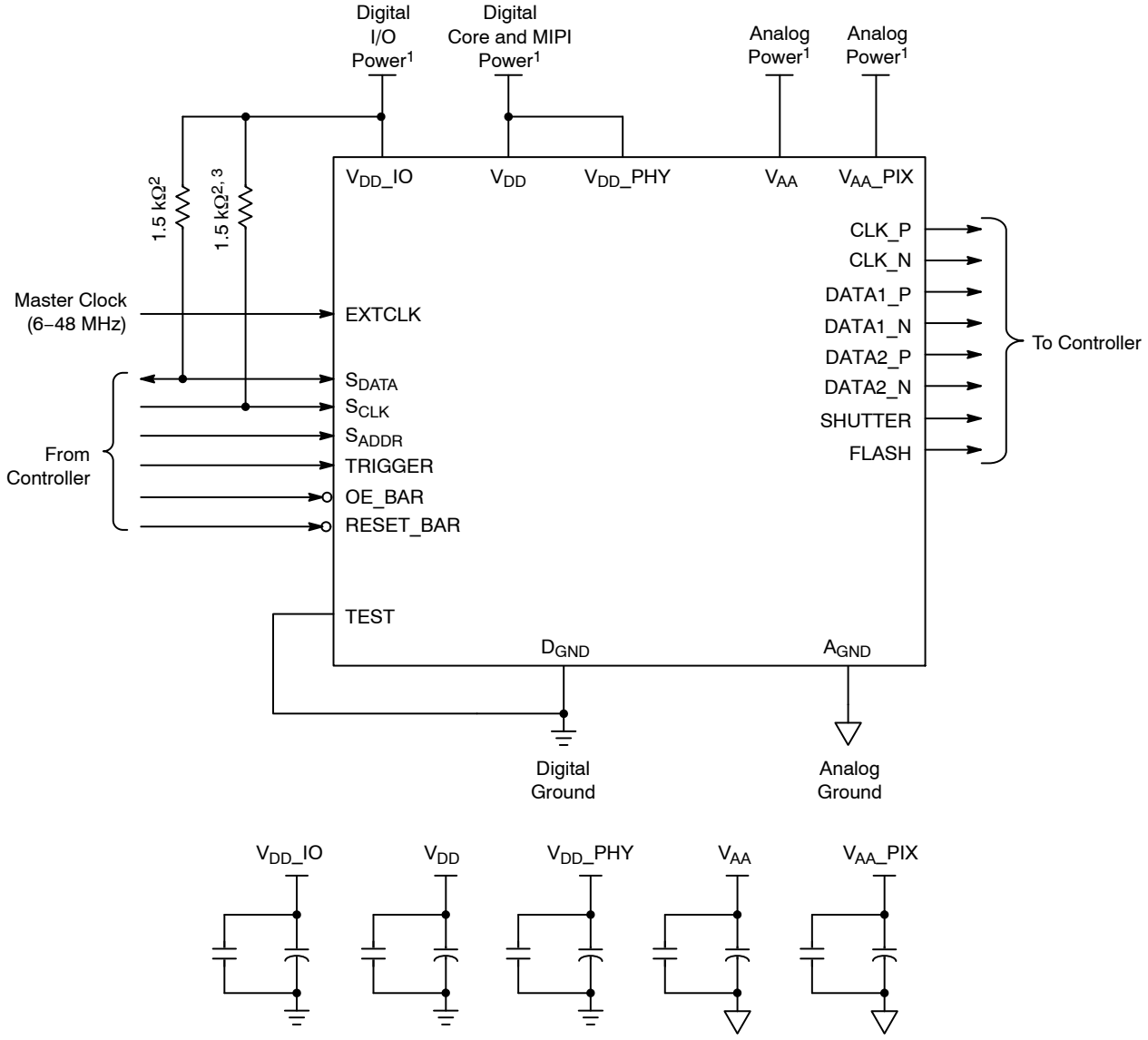
Figure 4. Pixel Mono Pattern Detail (Top Right Corner)

Default Readout Order

By convention, the sensor core pixel array is shown with the first addressable (logical) pixel (0,4) in the top right corner (see Figure 3). This reflects the actual layout of the array on the die. Also, the physical location of the first pixel data read out of the sensor in default condition is that of pixel (6,10).

CONFIGURATION AND PINOUT

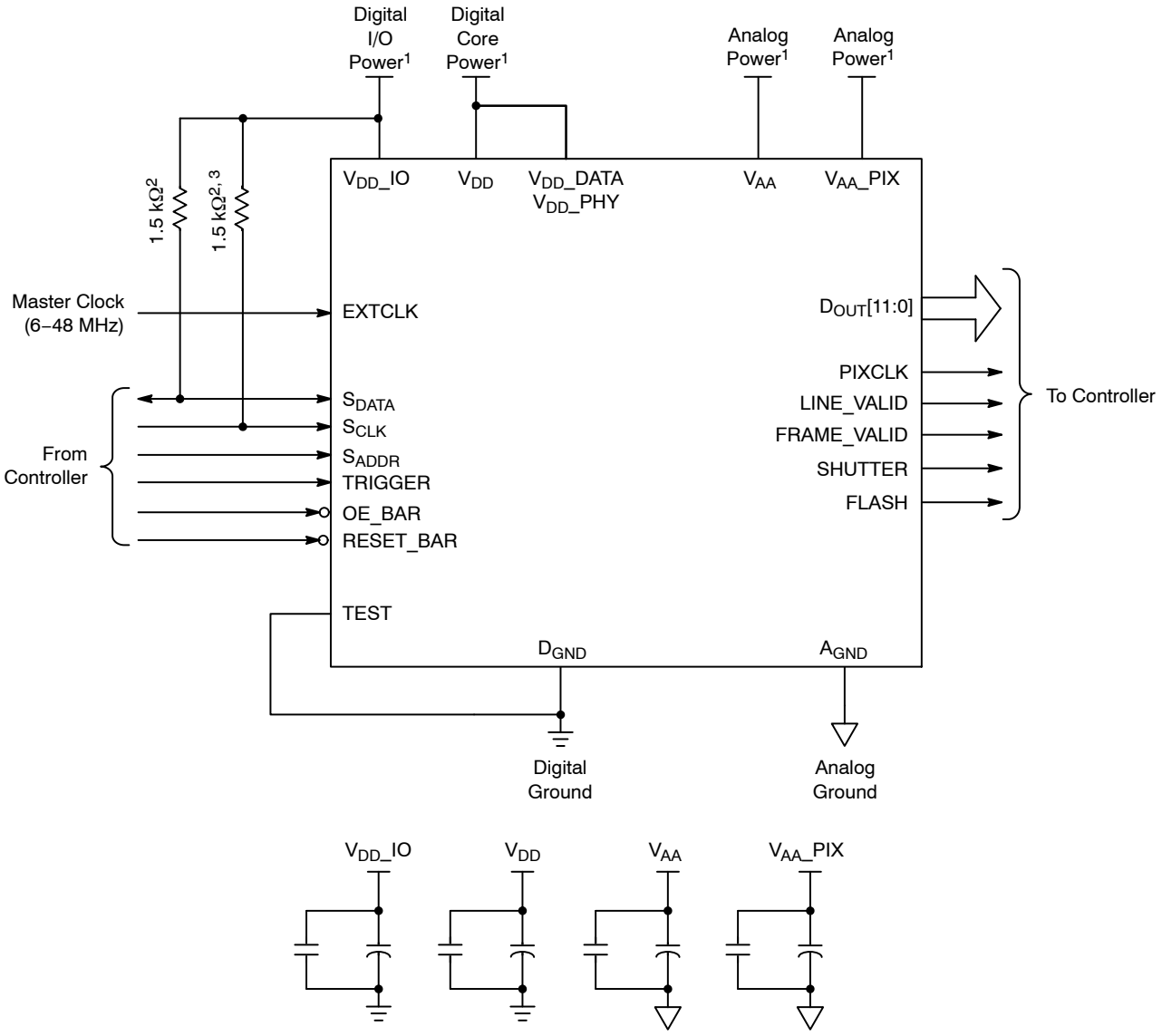
The figures and tables below show a typical configuration for the AR0144CS image sensor and show the package pinouts.



Notes:

1. All power supplies must be adequately decoupled.
2. ON Semiconductor recommends a resistor value of 1.5 kΩ, but a greater value may be used for slower two-wire speed.
3. This pull-up resistor is not required if the controller drives a valid logic level on S_{CLK} at all times.
4. The parallel interface output pads can be left unconnected if the serial output interface is used.
5. ON Semiconductor recommends that 0.1 μF and 10 μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on the layout and design considerations. Refer to the AR0144CS demo head-board schematics for circuit recommendations.
6. ON Semiconductor recommends that analog power planes be placed in a manner such that coupling with the digital power planes is minimized.

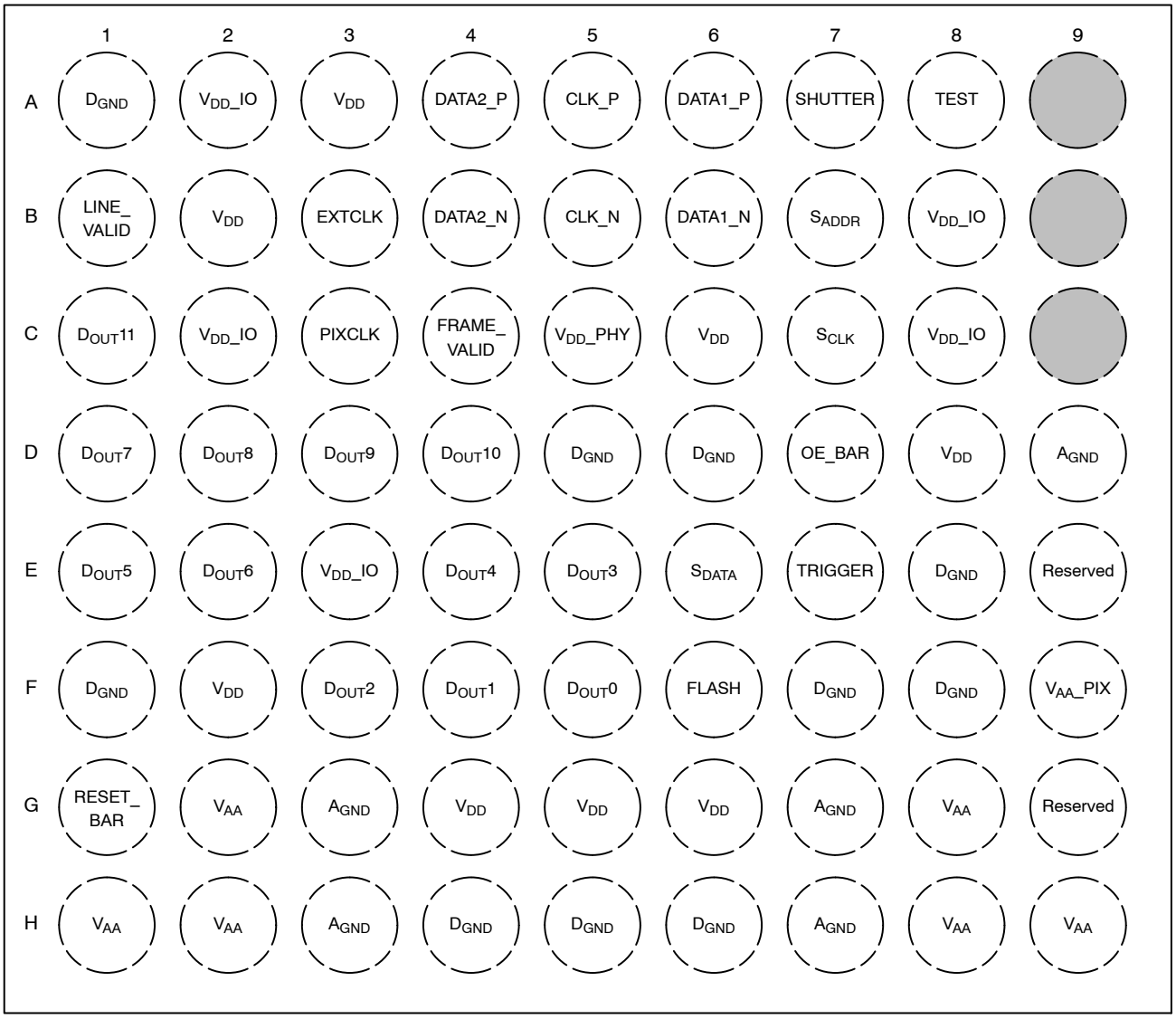
Figure 5. Serial 2-lane MIPI Interface



Notes:

1. All power supplies must be adequately decoupled.
2. ON Semiconductor recommends a resistor value of 1.5 kΩ, but a greater value may be used for slower two-wire speed.
3. This pull-up resistor is not required if the controller drives a valid logic level on S_{CLK} at all times.
4. The serial interface output pads can be left unconnected if the parallel output interface is used.
5. ON Semiconductor recommends that 0.1 μF and 10 μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on the layout and design considerations. Refer to the AR0144CS demo headboard schematics for circuit recommendations.
6. ON Semiconductor recommends that analog power planes be placed in a manner such that coupling with the digital power planes is minimized.

Figure 6. Parallel Pixel Data Interface



Top View
(Ball Down)

Figure 7. 5.546 × 5.565 mm 69-ball CSP Package

Table 3. PIN DESCRIPTIONS – 69-BALL CSP PACKAGE

Name	CSP Ball	Type	Description
DATA1_N	B6	Output	MIPI serial data, lane 1, differential N
DATA1_P	A6	Output	MIPI serial data, lane 1, differential P
DATA2_N	B4	Output	MIPI serial data, lane 2, differential N
DATA2_P	A4	Output	MIPI serial data, lane 2, differential P
CLK_N	B5	Output	MIPI serial clock differential N
CLK_P	A5	Output	MIPI serial clock differential P
V_{AA}	G2, G8, H1, H2, H8, H9	Power	Analog power
EXTCLK	B3	Input	External input clock
V_{DD}_PHY	C5	Power	MIPI power supply (1.2 V)

Table 3. PIN DESCRIPTIONS – 69-BALL CSP PACKAGE (continued)

Name	CSP Ball	Type	Description
D_{GND}	A1, D5, D6, E8, F1, F7, F8, H4, H5, H6	Power	Digital GND
V_{DD}	A3, B2, C6, D8, F2, G4, G5, G6	Power	Digital power
A_{GND}	D9, G3, G7, H3, H7	Power	Analog GND
S_{ADDR}	B7	Input	Two-Wire Serial address select
S_{CLK}	C7	Input	Two-Wire Serial clock input
S_{DATA}	E6	I/O	Two-Wire Serial data I/O
V_{AA}_PIX	F9	Power	Pixel power
LINE_VALID	B1	Output	Asserted when D_{OUT} line data is valid
FRAME_VALID	C4	Output	Asserted when D_{OUT} frame data is valid
PIXCLK	C3	Output	Pixel clock out. D_{OUT} is valid on rising edge of this clock
SHUTTER	A7	Output	Control of external mechanical shutter
FLASH	F6	Output	Control signal to drive external light sources
V_{DD}_IO	A2, B8, C2, C8, E3	Power	I/O supply power
D_{OUT}8	D2	Output	Parallel pixel data output
D_{OUT}9	D3	Output	Parallel pixel data output
D_{OUT}10	D4	Output	Parallel pixel data output
D_{OUT}11	C1	Output	Parallel pixel data output (MSB)
TEST	A8	Input	Manufacturing test enable pin (connect to D_{GND})
D_{OUT}4	E4	Output	Parallel pixel data output
D_{OUT}5	E1	Output	Parallel pixel data output
D_{OUT}6	E2	Output	Parallel pixel data output
D_{OUT}7	D1	Output	Parallel pixel data output
TRIGGER	E7	Input	Exposure synchronization input
OE_BAR	D7	Input	Output enable (active LOW)
D_{OUT}0	F5	Output	Parallel pixel data output (LSB)
D_{OUT}1	F4	Output	Parallel pixel data output
D_{OUT}2	F3	Output	Parallel pixel data output
D_{OUT}3	E5	Output	Parallel pixel data output
RESET_BAR	G1	Input	Asynchronous reset (active LOW). All settings are restored to factory default
Reserved	E9, G9	N/A	Reserved (do not connect)

TWO-WIRE SERIAL REGISTER INTERFACE

The two-wire serial interface bus enables read/write access to control and status registers within the AR0144CS.

The interface protocol uses a master/slave model in which a master controls one or more slave devices. The sensor acts as a slave device. The master generates a clock (S_{CLK}) that is an input to the sensor and is used to synchronize transfers. Data is transferred between the master and the slave on a bidirectional signal (S_{DATA}). S_{DATA} is pulled up to V_{DD_IO} off-chip by a 1.5 kΩ resistor. Either the slave or master device can drive S_{DATA} LOW – the interface protocol determines which device is allowed to drive S_{DATA} at any given time.

The protocols described in the two-wire serial interface specification allow the slave device to drive S_{CLK} LOW; the AR0144CS uses S_{CLK} as an input only and therefore never drives it LOW.

Protocol

Data transfers on the two-wire serial interface bus are performed by a sequence of low-level protocol elements:

- a (repeated) start condition
- a slave address/data direction byte
- an (a no) acknowledge bit
- a message byte
- a stop condition

The bus is idle when both S_{CLK} and S_{DATA} are HIGH. Control of the bus is initiated with a start condition, and the bus is released with a stop condition. Only the master can generate the start and stop conditions.

Start Condition

A start condition is defined as a HIGH-to-LOW transition on S_{DATA} while S_{CLK} is HIGH. At the end of a transfer, the master can generate a start condition without previously generating a stop condition; this is known as a “repeated start” or “restart” condition.

Stop Condition

A stop condition is defined as a LOW-to-HIGH transition on S_{DATA} while S_{CLK} is HIGH.

Data Transfer

Data is transferred serially, 8 bits at a time, with the MSB transmitted first. Each byte of data is followed by an acknowledge bit or a no-acknowledge bit. This data transfer mechanism is used for the slave address/data direction byte and for message bytes.

One data bit is transferred during each S_{CLK} clock period. S_{DATA} can change when S_{CLK} is LOW and must be stable while S_{CLK} is HIGH.

Slave Address/Data Direction Byte

Bits [7:1] of this byte represent the device slave address and bit [0] indicates the data transfer direction. A “0” in bit [0] indicates a WRITE, and a “1” indicates a READ. The default slave addresses used by the AR0144CS are 0x20 (write address) and 0x21 (read address) in accordance with the specification. Alternate slave addresses of 0x30 (write address) and 0x31 (read address) can be selected by enabling and asserting the S_{ADDR} input.

An alternate slave address can also be programmed through R0x31FC.

Message Byte

Message bytes are used for sending register addresses and register write data to the slave device and for retrieving register read data.

Acknowledge Bit

Each 8-bit data transfer is followed by an acknowledge bit or a no-acknowledge bit in the S_{CLK} clock period following the data transfer. The transmitter (which is the master when writing, or the slave when reading) releases S_{DATA}. The receiver indicates an acknowledge bit by driving S_{DATA} LOW. As for data transfers, S_{DATA} can change when S_{CLK} is LOW and must be stable while S_{CLK} is HIGH.

No-Acknowledge Bit

The no-acknowledge bit is generated when the receiver does not drive S_{DATA} LOW during the S_{CLK} clock period following a data transfer. A no-acknowledge bit is used to terminate a read sequence.

Typical Sequence

A typical READ or WRITE sequence begins by the master generating a start condition on the bus. After the start condition, the master sends the 8-bit slave address/data direction byte. The last bit indicates whether the request is for a read or a write, where a “0” indicates a write and a “1” indicates a read. If the address matches the address of the slave device, the slave device acknowledges receipt of the address by generating an acknowledge bit on the bus.

If the request was a WRITE, the master then transfers the 16-bit register address to which the WRITE should take place. This transfer takes place as two 8-bit sequences and the slave sends an acknowledge bit after each sequence to indicate that the byte has been received. The master then transfers the data as an 8-bit sequence; the slave sends an acknowledge bit at the end of the sequence. The master stops writing by generating a (re)start or stop condition.

If the request was a READ, the master sends the 8-bit write slave address/data direction byte and 16-bit register address, the same way as with a WRITE request. The master then generates a (re)start condition and the 8-bit read slave address/data direction byte, and clocks out the register data, eight bits at a time. The master generates an acknowledge bit after each 8-bit transfer. The slave’s internal register address is automatically incremented after every 8 bits are transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

Single READ from Random Location

This sequence (Figure 8) starts with a dummy WRITE to the 16-bit address that is to be used for the READ. The master terminates the WRITE by generating a restart condition. The master then sends the 8-bit read slave address/data direction byte and clocks out one byte of register data. The master terminates the READ by generating a no-acknowledge bit followed by a stop condition. Figure 8 shows how the internal register address maintained by the AR0144CS is loaded and incremented as the sequence proceeds.

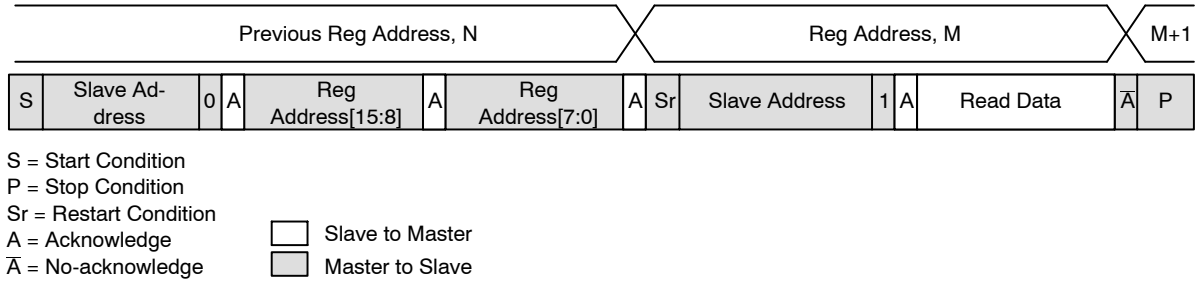


Figure 8. Single READ from Random Location

Single READ from Current Location

This sequence (Figure 9) performs a read using the current value of the AR0144CS internal register address. The master terminates the READ by generating a no-acknowledge bit followed by a stop condition. The figure shows two independent READ sequences.

Figure 9. Single READ from Current Location

Sequential READ, Start from Random Location

This sequence (Figure 10) starts in the same way as the single READ from random location (Figure 8). Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until “L” bytes have been read.

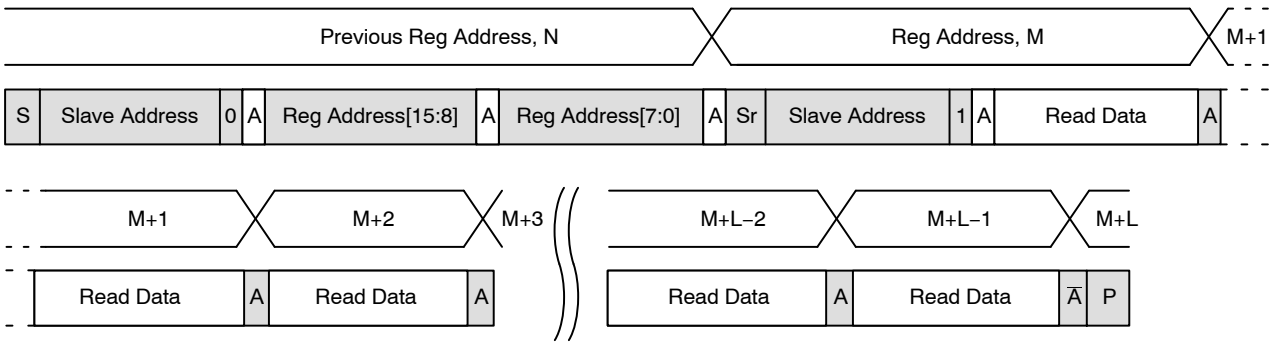


Figure 10. Sequential READ, Start from Random Location

Sequential READ, Start from Current Location

This sequence (Figure 11) starts in the same way as the single READ from current location (Figure 9). Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until “L” bytes have been read.

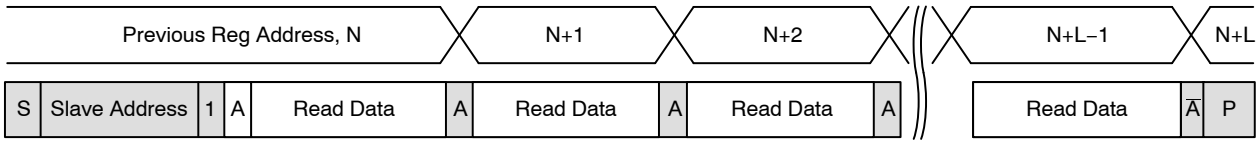


Figure 11. Sequential READ, Start from Current Location

Single WRITE to Random Location

This sequence (Figure 12) begins with the master generating a start condition. The slave address/data direction byte signals a WRITE and is followed by the HIGH then LOW bytes of the register address that is to be written. The master follows this with the byte of write data. The WRITE is terminated by the master generating a stop condition.

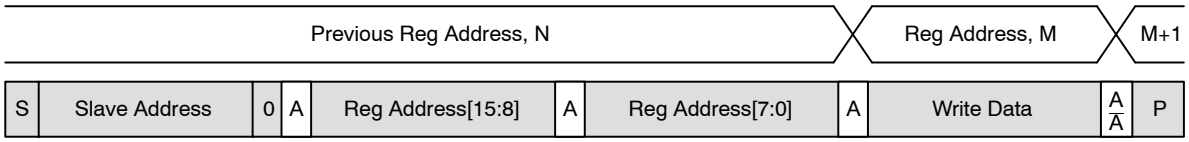


Figure 12. Single WRITE to Random Location

Sequential WRITE, Start at Random Location

This sequence (Figure 13) starts in the same way as the single WRITE to random location (Figure 12). Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte WRITEs until “L” bytes have been written. The WRITE is terminated by the master generating a stop condition.

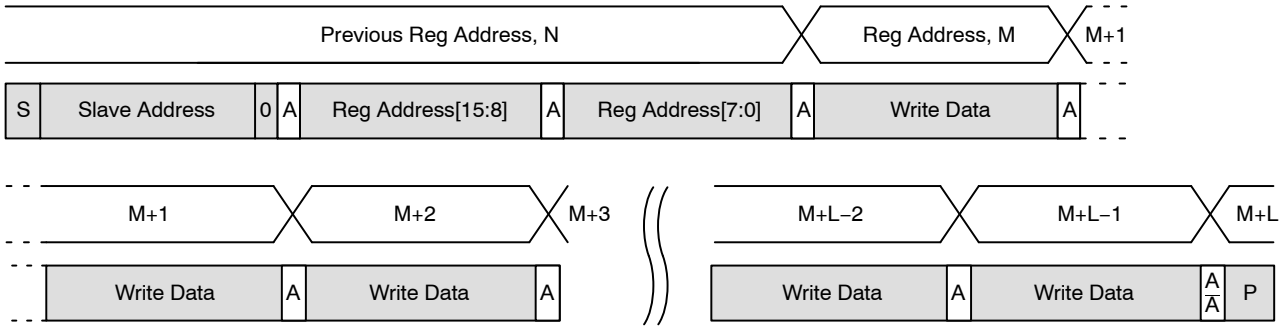


Figure 13. Sequential WRITE, Start at Random Location

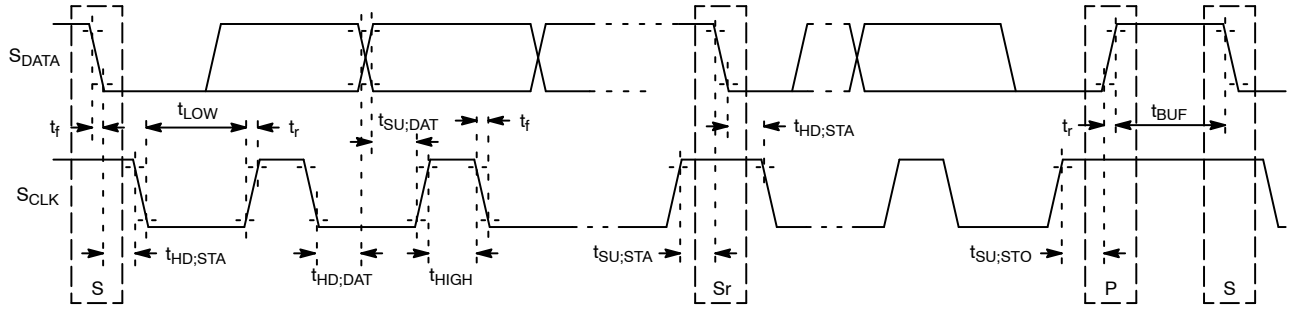
ELECTRICAL SPECIFICATIONS

Unless otherwise stated, the following specifications apply to the following conditions:

V_{DD} = V_{DD}_PHY = 1.2 V ±0.06;
V_{DD}_IO = V_{AA} = V_{AA}_PIX = 2.8 V ±0.3 V;
T_A = −40°C to +105°C;
Output Load = 10 pF;
PIXCLK Frequency = 74.25 MHz;
MIPI off.

Two-Wire Serial Register Interface

The electrical characteristics of the two-wire serial register interface (S_{CLK}, S_{DATA}) are shown in Figure 14 and Table 4.



NOTE: Read sequence: For an 8-bit READ, read waveforms start after WRITE command and register address are issued.

Figure 14. Two-Wire Serial Bus Timing Parameters

Table 4. TWO-WIRE SERIAL BUS CHARACTERISTICS

(f_{EXTCLK} = 27 MHz; V_{DD} = 1.2 V; V_{DD}_IO = 2.8 V; V_{AA} = 2.8 V; V_{AA}_PIX = 2.8 V; V_{DD}_PHY = 1.2 V; T_A = 25°C)

Parameter	Symbol	Standard Mode		Fast-Mode		Unit
		Min	Max	Min	Max	
S_{CLK} Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold Time (Repeated) START Condition	$t_{HD;STA}$	4.0	–	0.6	–	μs
LOW Period of the S_{CLK} Clock	t_{LOW}	4.7	–	1.3	–	μs
HIGH Period of the S_{CLK} Clock	t_{HIGH}	4.0	–	0.6	–	μs
Set-up Time for a Repeated START Condition	$t_{SU;STA}$	4.7	–	0.6	–	μs
Data Hold Time	$t_{HD;DAT}$	0 (Note 4)	3.45 (Note 5)	0 (Note 6)	0.9 (Note 5)	μs
Data Set-up Time	$t_{SU;DAT}$	250	–	100 (Note 6)	–	ns
Rise Time of both S_{DATA} and S_{CLK} Signals	t_r	–	1000	20 + 0.1Cb (Note 7)	300	ns
Fall Time of both S_{DATA} and S_{CLK} Signals	t_f	–	300	20 + 0.1Cb (Note 7)	300	ns
Set-up Time for STOP Condition	$t_{SU;STO}$	4.0	–	0.6	–	μs
Bus Free Time between a STOP and START Condition	t_{BUF}	4.7	–	1.3	–	μs
Capacitive Load for each Bus Line	Cb	–	400	–	400	pF
Serial Interface Input Pin Capacitance	CIN_SI	–	3.3	–	3.3	pF

Table 4. TWO-WIRE SERIAL BUS CHARACTERISTICS (continued)
(f_{EXTCLK} = 27 MHz; V_{DD} = 1.2 V; V_{DD}_IO = 2.8 V; V_{AA} = 2.8 V; V_{AA}_PIX = 2.8 V; V_{DD}_PHY = 1.2 V; T_A = 25°C)

Parameter	Symbol	Standard Mode		Fast-Mode		Unit
		Min	Max	Min	Max	
S_{DATA} Max Load Capacitance	CLOAD_SD	–	30	–	30	pF
S_{DATA} Pull-up Resistor	RSD	1.5	4.7	1.5	4.7	kΩ

1. This table is based on I²C standard (v2.1 January 2000). Philips Semiconductor.
2. Two-wire control is I²C-compatible.
3. All values referred to V_{IHmin} = 0.9 V_{DD}_IO and V_{ILmax} = 0.1 V_{DD}_IO levels. Sensor EXCLK = 27 MHz.
4. A device must internally provide a hold time of at least 300 ns for the S_{DATA} signal to bridge the undefined region of the falling edge of S_{CLK}.
5. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the S_{CLK} signal.
6. A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{SU;DAT}$ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the S_{CLK} signal. If such a device does stretch the LOW period of the S_{CLK} signal, it must output the next data bit to the S_{DATA} line t_r max + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the S_{CLK} line is released.
7. Cb = total capacitance of one bus line in pF.

I/O Timing

By default, the AR0144CS launches pixel data, FV and LV with the falling edge of PIXCLK. The expectation is that the user captures D_{OUT}[11:0], FV and LV using the rising edge of PIXCLK. The launch edge of PIXCLK can be configured in register R0x3028. See Figure 15 and Table 5 for I/O timing (AC) characteristics.

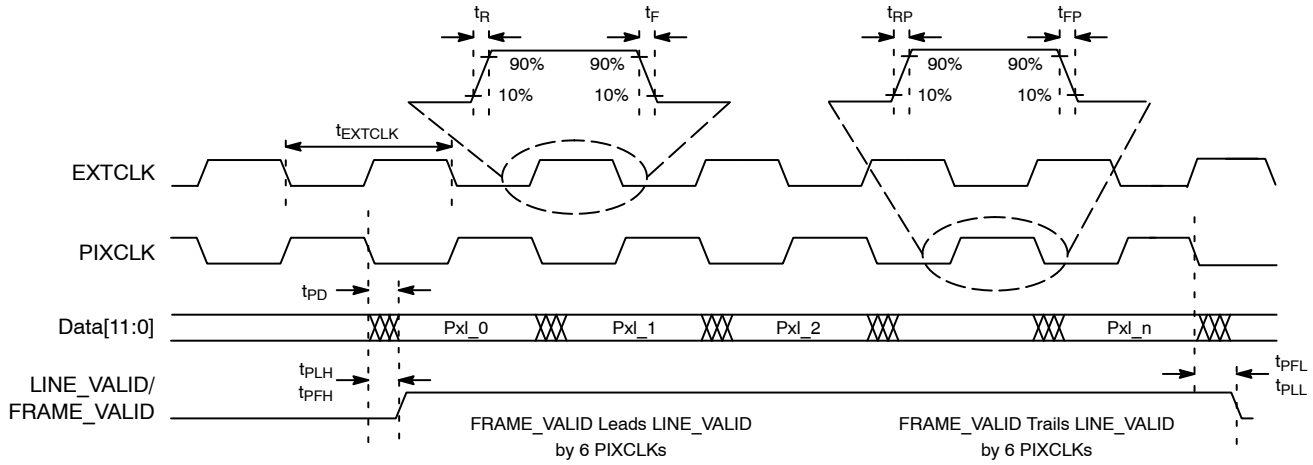


Figure 15. I/O Timing Diagram

Table 5. I/O TIMING CHARACTERISTICS, PARALLEL OUTPUT (1.8 V V_{DD_IO}) (Note 8)

Symbol	Definition	Condition	Min	Typ	Max	Unit
f_{EXTCLK}	Input Clock Frequency		6	–	48	MHz
t_{EXTCLK}	Input Clock Period		20.8	–	166	ns
t_R	Input Clock Rise Time	PLL Enabled	–	3	11.1 (Note 10)	ns
t_F	Input Clock Fall Time	PLL Enabled	–	3	11.1 (Note 10)	ns
t_{JITTER}	Input Clock Jitter		–	–	600	ps
t_{cp}	EXTCLK to PIXCLK Propagation Delay	Nominal Voltages, PLL Disabled, PIXCLK Slew Rate = 4	5.7	–	14.3	ns
t_{RP}	PIXCLK Rise Time	PCLK Slew Rate = 6	1.3	–	4.0	ns
t_{FP}	PIXCLK Fall Time	PCLK Slew Rate = 6	1.3	–	3.9	ns
	PIXCLK Duty Cycle		45	50	55	%
f_{PIXCLK}	PIXCLK Frequency	PIXCLK Slew Rate = 6, Data Slew Rate = 7	6	–	74.25	MHz
t_{PD}	PIXCLK to Data Valid	PIXCLK Slew Rate = 6, Data Slew Rate = 7	–2.5	–	2	ns
t_{PFH}	PIXCLK to FV HIGH	PIXCLK Slew Rate = 6, Data Slew Rate = 7	–2.5	–	2	ns
t_{PLH}	PIXCLK to LV HIGH	PIXCLK Slew Rate = 6, Data Slew Rate = 7	–3	–	1.5	ns
t_{PFL}	PIXCLK to FV LOW	PIXCLK Slew Rate = 6, Data Slew Rate = 7	–2.5	–	2	ns
t_{PLL}	PIXCLK to LV LOW	PIXCLK Slew Rate = 6, Data Slew Rate = 7	–3	–	1.5	ns
C_{IN}	Input Pin Capacitance		–	2.5	–	pF

8. Minimum and maximum values are taken at 105°C junction, 2.5 V and –40°C junction, 3.1 V. All values are taken at the 50% transition point. The loading used is 10 pF.
9. Jitter from PIXCLK is already taken into account in the data for all of the output parameters.
10. 11.1 ns is for 30% of 27 MHz external clock. For 24 MHz external clock, 30% of clock period is 12.5 ns.

Table 6. I/O TIMING CHARACTERISTICS, PARALLEL OUTPUT (2.8 V V_{DD_IO}) (Note 11)

Symbol	Definition	Condition	Min	Typ	Max	Unit
f_{EXTCLK}	Input Clock Frequency		6	–	48	MHz
t_{EXTCLK}	Input Clock Period		20.8	–	166	ns
t_R	Input Clock Rise Time	PLL Enabled	–	3	–	ns
t_F	Input Clock Fall Time	PLL Enabled	–	3	–	ns
t_{JITTER}	Input Clock Jitter		–	–	600	ps
t_{cp}	EXTCLK to PIXCLK Propagation Delay	Nominal Voltages, PLL Disabled, PIXCLK Slew Rate = 4	5.3	–	13.4	ns
t_{RP}	PIXCLK Rise Time	PCLK Slew Rate = 6	1.3	–	4.0	ns
t_{FP}	PIXCLK Fall Time	PCLK slew rate = 6	1.3	–	3.9	ns
	PIXCLK Duty Cycle		45	50	55	%
f_{PIXCLK}	PIXCLK Frequency	PIXCLK Slew Rate = 6, Data Slew Rate = 7	6	–	74.25	MHz
t_{PD}	PIXCLK to Data Valid	PIXCLK Slew Rate = 6, Data Slew Rate = 7	–2.5	–	2	ns
t_{PFH}	PIXCLK to FV HIGH	PIXCLK Slew Rate = 6, Data Slew Rate = 7	–2.5	–	2	ns
t_{PLH}	PIXCLK to LV HIGH	PIXCLK Slew Rate = 6, Data Slew Rate = 7	–2.5	–	2	ns
t_{PFL}	PIXCLK to FV LOW	PIXCLK Slew Rate = 6, Data Slew Rate = 7	–2.5	–	2	ns
t_{PLL}	PIXCLK to LV LOW	PIXCLK Slew Rate = 6, Data Slew Rate = 7	–2.5	–	2	ns
C_{IN}	Input Pin Capacitance		–	2.5	–	pF

11. Minimum and maximum values are taken at 105°C junction, 2.5 V and –40°C junction, 3.1 V. All values are taken at the 50% transition point. The loading used is 10 pF.
12. Jitter from PIXCLK is already taken into account in the data for all of the output parameters.

Table 7. I/O RISE SLEW RATE (2.8 V V_{DD}_IO) (Note 13)

Parallel Slew (R0x306E[15:13])	Min	Typ	Max	Unit
0	1.02	1.76	2.52	V/ns
1	1.2	2.05	3.14	V/ns
2	1.35	2.38	3.52	V/ns
3	1.57	2.72	4	V/ns
4	1.76	2.9	4.49	V/ns
5	1.87	3.16	4.88	V/ns
6	2.07	3.5	5.35	V/ns
7	2.22	3.75	5.77	V/ns

13. Minimum and maximum values are taken at 105°C junction, 2.5 V and −40°C junction, 3.1 V. The loading used is 10 pF.

Table 8. I/O FALL SLEW RATE (2.8 V V_{DD}_IO) (Note 14)

Parallel Slew (R0x306E[15:13])	Min	Typ	Max	Unit
0	0.8	1.33	2.01	V/ns
1	1.05	1.71	2.51	V/ns
2	1.28	2.14	3.07	V/ns
3	1.49	2.49	3.53	V/ns
4	1.64	2.75	4.05	V/ns
5	1.83	3.06	4.54	V/ns
6	2.01	3.38	4.86	V/ns
7	2.17	3.63	5.32	V/ns

14. Minimum and maximum values are taken at 105°C junction, 2.5 V and −40°C junction, 3.1 V. The loading used is 10 pF.

Table 9. I/O RISE SLEW RATE (1.8 V V_{DD}_IO) (Note 15)

Parallel Slew (R0x306E[15:13])	Min	Typ	Max	Unit
0	0.386	0.61	1.05	V/ns
1	0.459	0.727	1.24	V/ns
2	0.528	0.849	1.41	V/ns
3	0.595	0.944	1.59	V/ns
4	0.662	1.06	1.77	V/ns
5	0.728	1.14	1.94	V/ns
6	0.792	1.26	2.11	V/ns
7	0.855	1.38	2.27	V/ns

15. Minimum and maximum values are taken at 105°C junction, 1.7 V and −40°C junction, 1.95 V. The loading used is 10 pF.

Table 10. I/O FALL SLEW RATE (1.8 V V_{DD}_IO) (Note 16)

Parallel Slew (R0x306E[15:13])	Min	Typ	Max	Unit
0	0.33	0.546	0.888	V/ns
1	0.43	0.713	1.16	V/ns
2	0.51	0.853	1.41	V/ns
3	0.6	1.02	1.64	V/ns
4	0.7	1.15	1.86	V/ns
5	0.77	1.3	2.04	V/ns
6	0.86	1.41	2.26	V/ns
7	0.94	1.51	2.43	V/ns

16. Minimum and maximum values are taken at 105°C junction, 1.7 V and −40°C junction, 1.95 V. The loading used is 10 pF.

DC Electrical Characteristics

The DC electrical characteristics are shown in Table 11, Table 12, Table 13, and Table 15.

Table 11. DC ELECTRICAL CHARACTERISTICS

Symbol	Definition	Condition	Min	Typ	Max	Unit
V_{DD}	Core Digital Voltage		1.14	1.2	1.26	V
V_{DD_IO}	I/O Digital Voltage		1.7/2.5	1.8/2.8	1.9/3.1	V
V_{AA}	Analog Voltage		2.5	2.8	3.1	V
V_{AA_PIX}	Pixel Supply Voltage		2.5	2.8	3.1	V
V_{DD_PHY}	MIPI Supply Voltage		1.14	1.2	1.26	V
V_{IH}	Input HIGH Voltage		V_{DD_IO} * 0.7	–		V
V_{IL}	Input LOW Voltage		–	–	V_{DD_IO} * 0.3	V
I_{IN}	Input Leakage Current	No Pull-up Resistor; V_{IN} = V_{DD_IO} or D_{GND}	–	–	20	μA
V_{OH}	Output HIGH Voltage		V_{DD_IO} – 0.3	–	–	V
V_{OL}	Output LOW Voltage	V_{DD_IO} = 2.8 V	–	–	0.4	V
I_{OH}	Output HIGH Current	At Specified V_{OH}	–12 (Note 17)	–	–	mA
I_{OL}	Output LOW Current	At Specified V_{OL}	–	–	12 (Note 17)	mA

17. A slew rate setting of 7 is needed to acheive IOH and IOL minimum and maximum specifications.

CAUTION: Stresses greater than those listed in Table 12 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Table 12. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Minimum	Maximum	Unit
V_{SUPPLY}	Power Supply Voltage (All Supplies)	–0.3	4.5	V
I_{SUPPLY}	Total Power Supply Current	–	200	mA
I_{GND}	Total Ground Current	–	200	mA
V_{IN}	DC Input Voltage	–0.3	V_{DD_IO} + 0.3	V
V_{OUT}	DC Output Voltage	–0.3	V_{DD_IO} + 0.3	V
T_{STG}	Storage Temperature (Note 18)	–40	+150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

18. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 13. OPERATING CURRENT CONSUMPTION FOR PARALLEL OUTPUT

(V_{AA} = V_{AA_PIX} = V_{DD_IO} = 2.8 V; V_{DD} = V_{DD_PHY} = 1.2 V; PLL Enabled and PIXCLK = 74.25 MHz; T_A = 25°C; C_{LOAD} = 10 pF)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{DD}	Digital Operating Current	Parallel, Streaming, Full Resolution 60 fps	–	41	51	mA
I_{DD_IO}	I/O Digital Operating Current	Parallel, Streaming, Full Resolution 60 fps	–	24	NA (Note 20)	mA
I_{AA}	Analog Operating Current	Parallel, Streaming, Full Resolution 60 fps	–	31	37	mA
I_{AA_PIX}	Pixel Supply Current	Parallel, Streaming, Full Resolution 60 fps	–	3	3.5	mA

19. V_{DD_PHY} is shorted internally in the part. The external supply to V_{DD} and V_{DD_PH} should be the same supply.
20. Maximum values for V_{DD_IO} parallel are dependent on the specific load being applied in the final design. Typical values are based on a load of 20 pF.

Table 14. OPERATING CURRENT CONSUMPTION FOR MIPI OUTPUT

(V_{AA} = V_{AA}_PIX = V_{DD}_IO = 2.8 V; V_{DD} = V_{DD}_PHY = 1.2 V; PLL Enabled and PIXCLK = 74.25 MHz; T_A = 25°C; C_{LOAD} = 10 pF)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{DD}	Digital Operating Current	MIPI, Streaming, Full Resolution 60 fps	–	55	82	mA
I_{DD}_IO	I/O Digital Operating Current	MIPI, Streaming, Full Resolution 60 fps	–	0.15	0.35	mA
I_{AA}	Analog Operating Current	MIPI, Streaming, Full Resolution 60 fps	–	30	36	mA
I_{AA}_PIX	Pixel Supply Current	MIPI, Streaming, Full Resolution 60 fps	–	3	3.5	mA

21. V_{DD}_PHY is shorted internally in the part. The external supply to V_{DD} and V_{DD}_PH should be the same supply.

Table 15. STANDBY CURRENT CONSUMPTION

(Analog = V_{AA} + V_{AA}_PIX + V_{DD}_IO; Digital = V_{DD} + V_{DD}_PHY; T_A = 25°C)

Definition	Condition	Min	Typ	Max	Unit
Hard Standby (Clock Off, Driven Low)	Analog, 2.8 V	–	15	200	μA
	Digital, 1.2 V	–	270	1500	μA
Hard Standby (Clock On, EXTCLK = 20 MHz)	Analog, 2.8 V	–	15	200	μA
	Digital, 1.2 V	–	270	1500	μA
Soft Standby (Clock Off, Driven Low)	Analog, 2.8 V	–	15	200	μA
	Digital, 1.2 V	–	270	1500	μA
Soft Standby (Clock On, EXTCLK = 20 MHz)	Analog, 2.8 V	–	70	240	μA
	Digital, 1.2 V	–	2600	5400	μA

POWER-ON RESET AND STANDBY TIMING

Power-Up Sequence

The recommended power-up sequence for the AR0144CS is shown in Figure 16. The available power supplies (V_{DD}_IO, V_{DD}, V_{DD}_PHY, V_{AA}, V_{AA}_PIX) must have the separation specified below.

1. Turn on V_{AA} and V_{AA}_PIX power supplies.
2. After 0–10 μs, turn on V_{DD}_IO power supply.
3. After 0–10 μs, turn on V_{DD}_PHY and V_{DD} power supplies.
4. After the last power supply is stable, enable EXTCLK.
5. If RESET_BAR is in a LOW state, hold RESET_BAR LOW for at least 1 ms.
   If RESET_BAR is in a HIGH state, bring RESET_BAR LOW for at least 1 ms.
6. Wait 160000 EXTCLKs (for internal initialization into software standby).
7. Configure PLL, output, and image settings to desired values.
8. Wait 1 ms for the PLL to lock.
9. Set streaming mode (R0x301a[2] = 1).

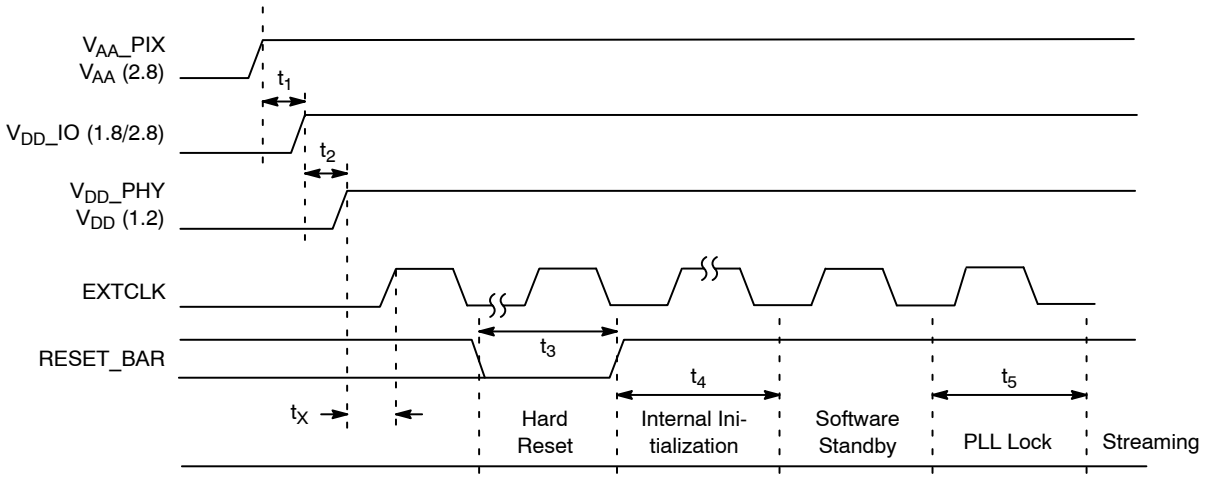


Figure 16. Power Up

Table 16. POWER-UP SEQUENCE

Symbol	Definition	Min	Typ	Max	Unit
t_1	V_{AA}/V_{AA}_PIX to V_{DD}_IO	0	10	–	μs
t_2	V_{DD}_IO to V_{DD}/V_{DD}_PHY	0	10	–	μs
t_X	Xtal Settle Time	–	30 (Note 22)	–	ms
t_3	Hard Reset	1 (Note 23)	–	–	ms
t_4	Internal Initialization	160000	–	–	EXTCLKs
t_5	PLL Lock Time	1	–	–	ms

22. Xtal settling time is component-dependent, usually taking about 10–100 ms.
23. Hard reset time is the minimum time required after power rails are settled. In a circuit where hard reset is held down by RC circuit, then the RC time must include the all power rail settle time and Xtal settle time.

Power-Down Sequence

The recommended power-down sequence for the AR0144CS is shown in Figure 17. The available power supplies (V_{DD}_IO, V_{DD}, V_{DD}_PHY, V_{AA}, V_{AA}_PIX) must have the separation specified below.

1. Disable streaming if output is active by setting standby R0x301a[2] = 0.
2. The soft standby state is reached after the current row or frame, depending on configuration, has ended.
3. Turn off V_{DD}_PHY/V_{DD}.
4. Turn off V_{DD}_IO.
5. Turn off V_{AA}/V_{AA}_PIX.

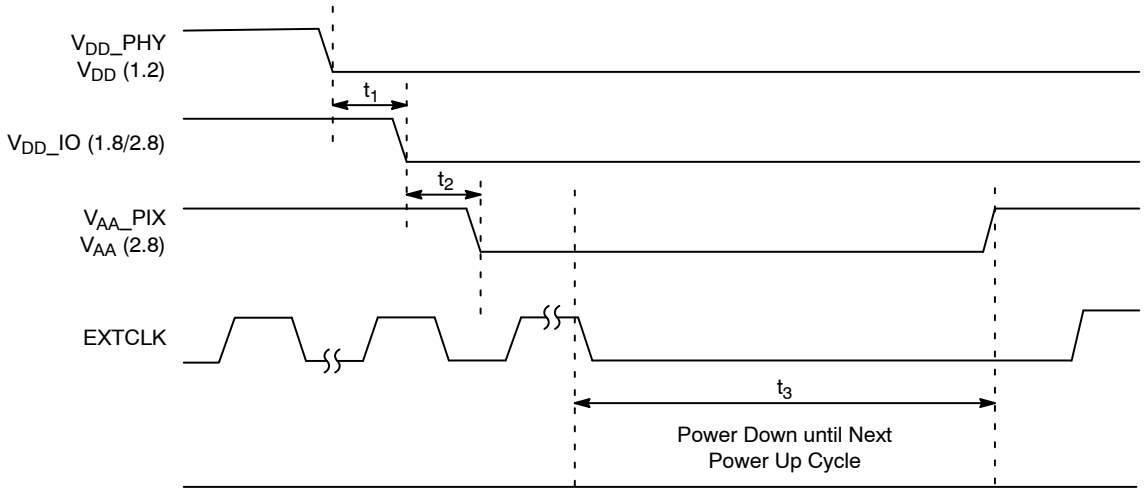


Figure 17. Power Down

Table 17. POWER-DOWN SEQUENCE

Symbol	Parameter	Min	Typ	Max	Unit
t_1	V_{DD}_PHY/V_{DD} to V_{DD}_IO	0	–	–	µs
t_2	V_{DD}_IO to V_{AA}/V_{AA}_PIX	0	–	–	µs
t_3	PwrDn until Next PwrUp Time (Note 24)	100	–	–	ms

24. t_3 is required between power down and next power up time; all decoupling caps from regulators must be completely discharged.

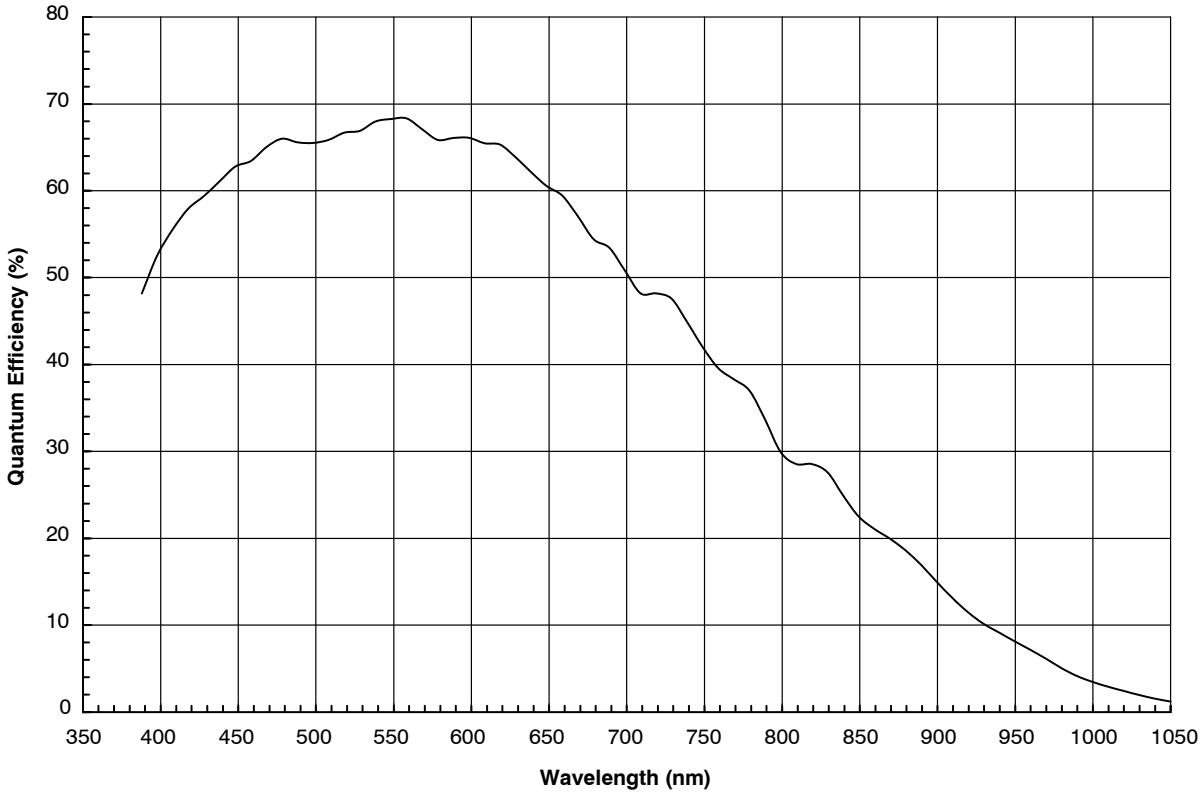


Figure 18. Quantum Efficiency – Monochrome Sensor (Typical)

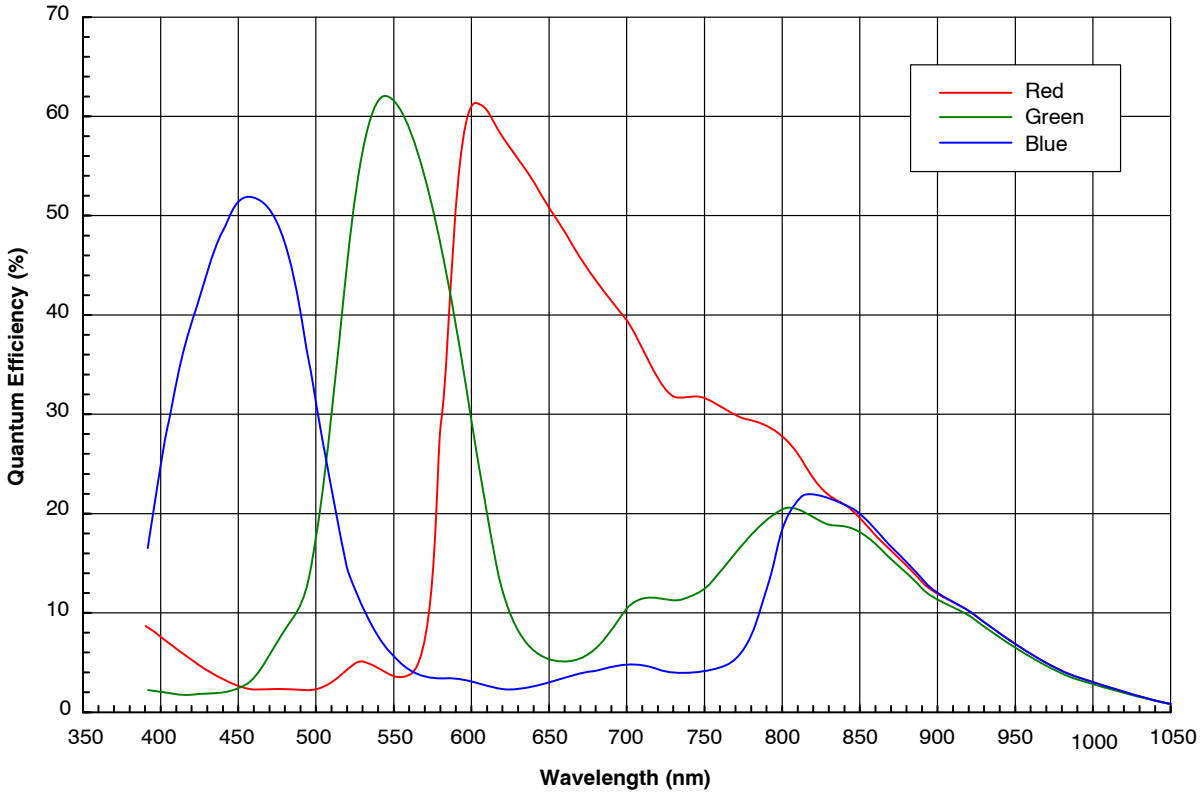


Figure 19. Quantum Efficiency – Color Sensor (Typical)

CRA vs. Image Height Plot

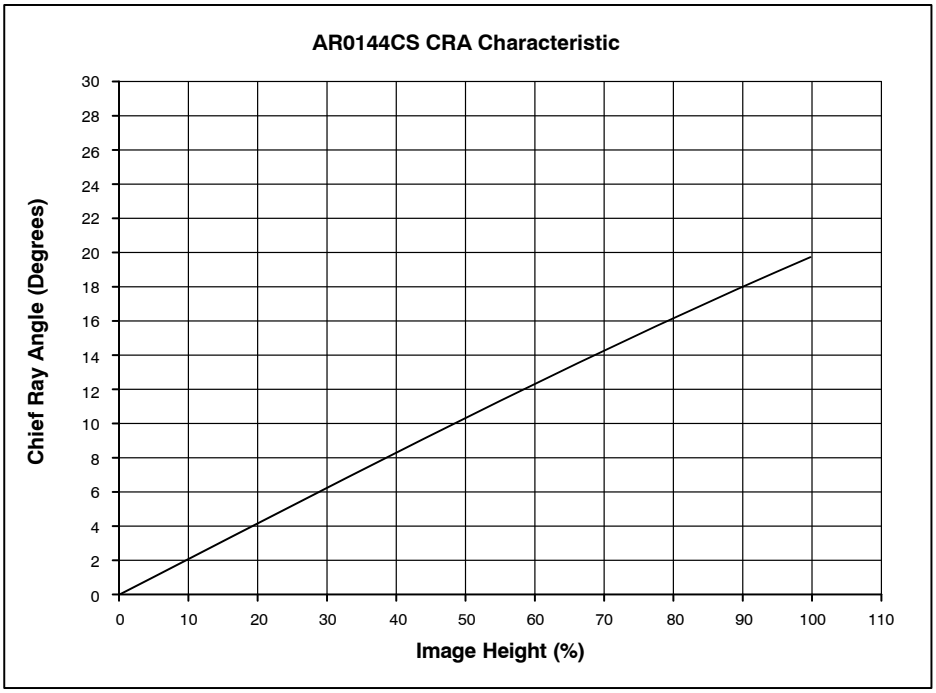


Figure 20. Chief Ray Angle – 20°

Image Height		CRA
(%)	(mm)	(deg)
0	0	0
5	0.113	1.02
10	0.226	2.03
15	0.340	3.05
20	0.453	4.07
25	0.566	5.08
30	0.679	6.10
35	0.792	7.10
40	0.906	8.11
45	1.019	9.11
50	1.132	10.11
55	1.245	11.11
60	1.358	12.10
65	1.472	13.08
70	1.585	14.05
75	1.698	15.02
80	1.811	15.98
85	1.925	16.94
90	2.038	17.88
95	2.151	18.82
100	2.264	19.74

CRA vs. Image Height Plot

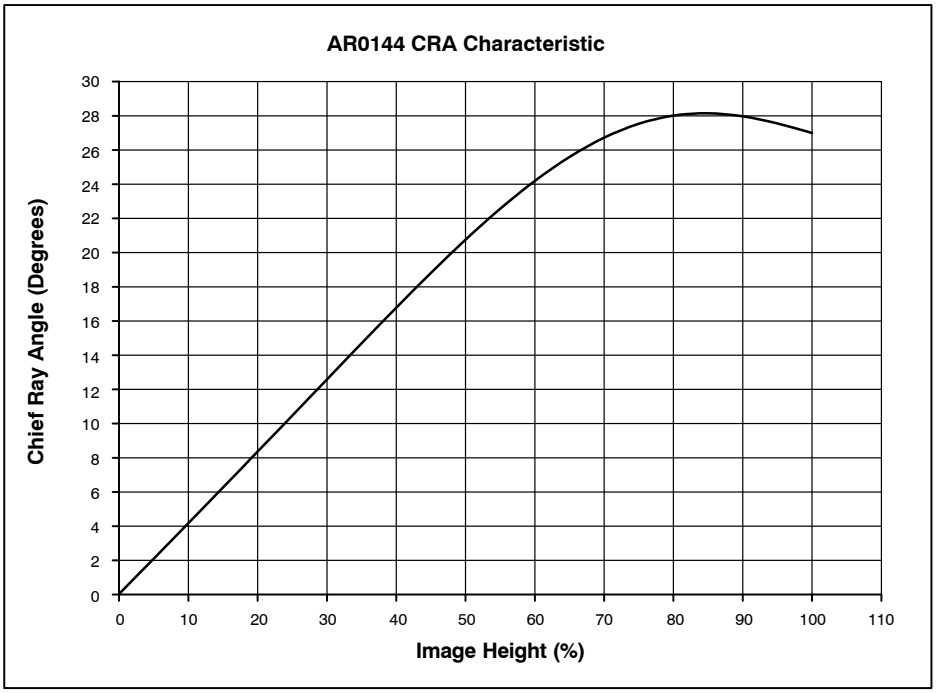
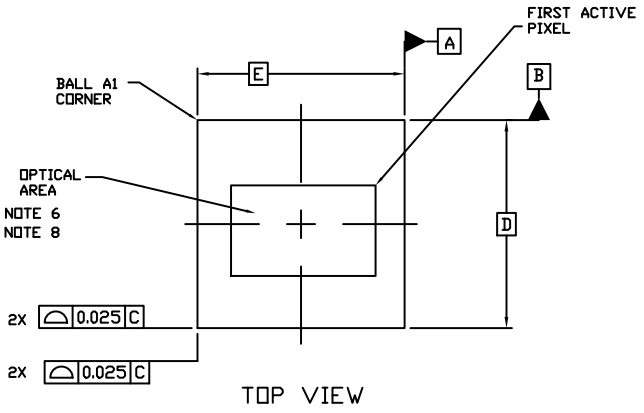


Figure 21. Chief Ray Angle – 28°

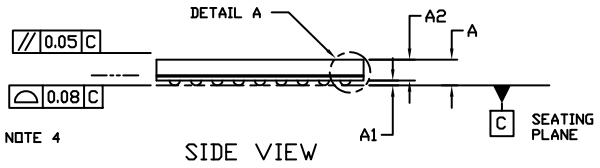
Image Height		CRA
(%)	(mm)	(deg)
0	0	0
5	0.113	2.07
10	0.226	4.15
15	0.340	6.24
20	0.453	8.34
25	0.566	10.45
30	0.679	12.56
35	0.792	14.68
40	0.906	16.76
45	1.019	18.80
50	1.132	20.74
55	1.245	22.55
60	1.358	24.19
65	1.472	25.59
70	1.585	26.72
75	1.698	27.53
80	1.811	28.01
85	1.925	28.14
90	2.038	27.97
95	2.151	27.55
100	2.264	27.00

ODCSP69 5.545x5.565
CASE 570BV
ISSUE B

DATE 02 MAY 2018



TOP VIEW

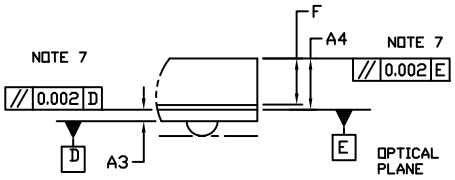


SIDE VIEW

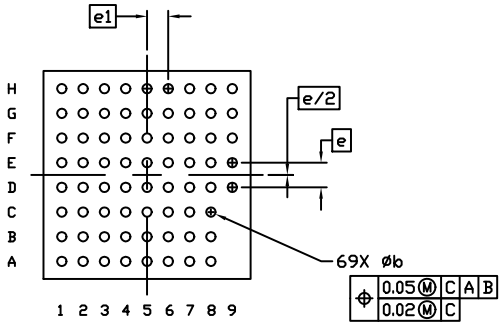
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM C.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPERICAL CROWNS OF THE SOLDER BALLS.
6. MAXIMUM ROTATION OF OPTICAL AREA RELATIVE TO D AND E WILL BE 0.1°. OPTICAL AREA IS DEFINED BY THE ACTIVE PIXEL ARRAY. REFER TO THE DEVICE DATASHEET FOR TOTAL ARRAY AND FIRST ACTIVE PIXEL DEFINITIONS.
7. PARALLELISM APPLIES ONLY TO THE OPTICAL AREA.
8. OPTICAL CENTER OFFSET WITH RESPECT TO THE PACKAGE CENTER IS X=62 MICRONS, Y=−171 MICRONS ±25 MICRONS.

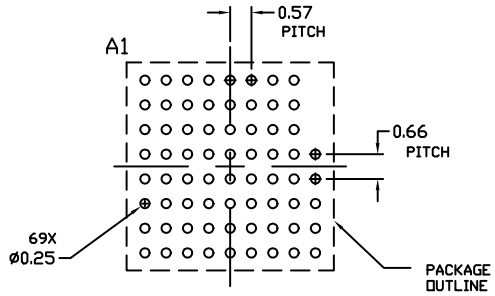
DIM	MILLIMETERS	
	MIN.	MAX.
A	---	0.77
A1	0.10	0.16
A2	0.56 REF	
A3	0.090	0.140
A4	0.425	0.465
b	0.22	0.28
D	5.565 BSC	
E	5.545 BSC	
e	0.66 BSC	
e1	0.57 BSC	
F	0.38	0.42



DETAIL A



BOTTOM VIEW



RECOMMENDED MOUNTING FOOTPRINT

DOCUMENT NUMBER:	**98AON07729G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**ODCSP69 5.545x5.565**		**PAGE 1 OF 1**

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

ON Semiconductor Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

◊